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- Gary Stringham
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- Mike Trimborn
- Joe Tykowski
- Mark Vanfleet

- Thomas Herbert
- Joseph Jacob
- Ton Janssen
- David Kalinsky
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The Embedded Training Program 2005 Classes

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ETP-203 Programmable Embedded Peripherals Simplify Complex Tasks

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ETP-226 Introduction to Posix Threads

ETP-227 Basic Control Theory for the Software Engineer

ETP-228 Introduction to the ANSI/EIA/CEA-709.1 Control Networking Protocol

ETP-229 Wireless Protocol Stacks

ETP-230 Top Ten Usability Mistakes

ETP-240 Inside Real-Time Kernels, Part 1

ETP-241 Design Patterns for Tasks in Real-Time Systems

ETP-242 SysML: The New Systems Modeling Language

ETP-243 Embedded Systems Programming Using DSPs

ETP-244 The 25 Most Common Mistakes with Real-Time Software Development, Part 1

ETP-245 Embedded Linux Startup Code

ETP-246 Memory Management, Part 1

ETP-247 PID without a PhD

ETP-248 Managing Power, Ground, and Noise in Microcontroller and Analog Applications

ETP-249 Understanding and Using the 802.11 Standards

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ETP-261 Executable UML
ETP-262 Leveraging Bit-Stream Encryption to Protect IP and Proprietary Designs
ETP-263 Embedded Systems Development: A Cookbook Approach
ETP-264 The 25 Most Common Mistakes with Real-Time Software Development, Part 2
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ETP-266 Memory Management, Part 2
ETP-267 Building Signaling Platforms with ATCA
ETP-268 An Introduction to eCos
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ETP-301 Writing Your First WinCE USB Device Driver
ETP-302 DODAF and the UML
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ETP-306 Optimizing C for Embedded Systems
ETP-307 Internet Messaging and Mail Protocols
ETP-308 IP Version 6 and the Dual Stack
ETP-309 Designing with Soft Processor Cores in FPGAs, Part 1
ETP-310 How to Streamline Embedded Systems Development with Eclipse
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ETP-367 FPGA Embedded Processors: Revealing True System Performance
ETP-368 Power Optimization Techniques for Embedded Systems Programmers
ETP-369 Using ZigBee Technology for Low Power Device Designs
ETP-370 CANopen-Based Transducer Network

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ETP-404 Selecting Linux as an Embedded Operating System
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ETP-406 Practical Statecharts for Embedded Systems, Part 1
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ETP-409 Hardware As Software: Designing with Configurable Processors
ETP-410 Establishing Great Software Development Process(es) for Your Organization
ETP-420 Real-Time Architectures: Past, Present, and Future, Part 1
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ETP-426 Practical Statecharts for Embedded Systems, Part 2
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ETP-428 Safety-Relevant Communication in Embedded Control Systems
ETP-429 Integrating the Trusted Platform Module into Embedded Systems
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ETP-440 Real-Time Architectures: Past, Present, and Future, Part 2
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Systems

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ETP-446 Data Management for Highly Available Embedded Systems

ETP-447 Covering Multiple Embedded Networking Technologies with CANopen

ETP-448 Building Internet Applications with Microsoft's .NET Compact Framework

ETP-449 Application Development for ZigBee Wireless Networking

ETP-450 The Hardware/Software Co-design for Road Vehicle Control System

ETP-460 Complementing DSPs with FPGAs

ETP-461 Scalable and Platform Agnostic Device Driver Architecture

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ETP-463 Integrating DSP Design and Test for Rapid Product Development

ETP-464 Power Management Strategies in Embedded Applications, Part 2

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ETP-470 Safety Critical Software Verification: Lessons From the DO-178B Approach



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Doug Abbott

Principal Consultant
Intellimetrix

Doug Abbott is an independent consultant with more than 30 years experience in embedded systems hardware and software design. He got his start back in the days when men were men and computers were more than wimpy little boxes sitting on the desktop. Having spent several years working with various real-time operating systems, he recently decided to jump on the Linux bandwagon. In addition to solving firmware problems for clients, Doug is a popular instructor leading seminars on real-time programming and other facets of embedded system design. He's also the author of two books: Linux for Embedded and Real-time Applications and PCI Bus Demystified. Abbott received his MSEE from UC Berkeley.

Classes:

ETP-201 - Linux 101

ETP-226 - Introduction to Posix Threads



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Jon Adams

Director of Radio Technology for the Wireless
Freescale Semiconductor, Inc.

Jon Adams has over 20 years of experience in the high technology industry. Prior to Motorola, Jon spent 17 years as a rocket scientist where he was part of the team involved with developing and deploying the Mars Network. During this time, Adams received several awards including the NASA Achievement Award (for years 1986, 1992 and 2000) and the JPL Award for Excellence. His current focus is the chipset/platform for a new IEEE protocol called 802.15.4, and the network layer atop that standard called ZigBee. Adams is also an expert on wireless communication technologies such as Ultra Wideband and Bluetooth, and has spoken frequently on both.

Classes:

[ETP-369 - Using ZigBee Technology for Low Power Device](#)

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Michael Anderson

Chief Scientist
The PTR Group, Inc.

Mike Anderson is Chief Scientist for The PTR Group, Inc. His background encompasses over 25 years of computer experience ranging from supercomputers to embedded 8-bit microprocessors. He is a former chairman of the VxWorks User's Group and has authored several courses and magazine articles designed to teach real-time and embedded systems programming. Anderson holds a BA in Mathematics from the University of South Florida and an MSCS from George Mason University.

Classes:

ETP-424 - Bringing up a Custom Linux BSP



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Bonnie Baker

Analog Applications Manager
Microchip Technology Inc.

Bonnie Baker has been involved with analog design and analog systems for nearly 20 years, having started as a manufacturing product engineer supporting analog products at Burr-Brown. From there, Baker moved up to IC design, analog division strategic marketer, and then corporate applications engineering manager. In 1998, she joined Microchip Technologys microperipherals division as the analog/mixed signal applications engineering manager. This has expanded her background to not only include analog applications, but to the microcontroller. Baker holds a MSEE from the University of Arizona and a bachelors degree in music education from Northern Arizona University. In addition to her fascination with analog design, Baker has a drive to share her knowledge and experience and has written more than 100 articles, design notes, and application notes and she is a frequent presenter at technical conferences and shows.

Classes:

ETP-248 - Managing Power, Ground, and Noise in Microcontroller and Analog Applications

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Michael Barr

President
Netrino, LLC

Michael Barr is the President of the Netrino Consultants Network. He has been an editor of Embedded Systems Programming since 1999 and a contributor since 1997. His book about embedded software development - Programming Embedded Systems in C and C++ (O'Reilly, 1999) - has taught tens of thousands of engineers the subject and been translated into several languages. He is also the author, with Jack Ganssle, of CMP Book's Embedded Systems Dictionary (2003).

Classes:

ETP-205 - Embedded Programming 101, Part 1
ETP-225 - Embedded Programming 101, Part 2

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Bill Beckwith

CTO

Objective Interface Systems

Bill Beckwith has been engineering software for over two decades with the last decade focused on embedded and real-time systems. He is the CTO of Objective Interface Systems, Inc. He is frequent speaker on real-time, embedded and high-assurance software in North America, Japan and Europe. Beckwith is currently involved in both developing software and standards for high-assurance embedded systems. He continues to lead the initiative for the advancement of CORBA and MILS in the real-time and embedded communities. Beckwith has served as an active author and editor of many standards including Real-time CORBA, Dynamic Scheduling and MILS protection profiles. Prior to objective Interface, he held management, engineering, and business development positions with Interbase Software, Systems Center, UCCEL, STSC, and MCI.

Classes:

ETP-465 - Secure Safety-Critical Distributed Embedded Systems



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Rich Blomseth

Product Manager
Echelon

Rich Blomseth is Echelon's Product Manager responsible for Web servers, IP routers, development and integration tools, and ANSI/EIA/CEA-709.1 open standards. He has been involved with embedded systems since 1978 when he was the U.S. Air Force's program manager directing more than 200 engineers developing the ground control system of the GPS satellite navigation system. He holds an MSCS, BSEE and BSCS from the University of California, Berkeley.

Classes:

ETP-228 - Introduction to the ANSI/EIA/CEA-709.1 Control Networking Protocol



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Thomas A. Bullinger

President
ArchSynergy, Ltd.

Tom Bullinger is founder and principal architect with ArchSynergy, a company devoted to software architecture. Bullinger developed his first embedded system in 1984, and has since worked on projects spanning the embedded domain, the desktop, and enterprise applications.

Throughout his career, his focus has been the practical application of process, architecture and object technology. Bullinger is also an Adjunct Professor at Rochester Institute of Technology, teaching courses in Computer Science and Software Engineering.

Classes:

ETP-263 - Embedded Systems Development: A Cookbook Approach



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Robert Burdick

Software Engineer
wAppearances

Mr. Burdick has extensive experience with a variety of wireless client technologies such as Windows CE, Windows CE .NET, and J2ME. His talents have been successfully utilized by Hewlett-Packard, Microsoft, Philips, and other leading technology companies. He is the author of Essential Windows CE Application Programming published by John Wiley and Sons. He is also co-author of Professional JSP, 2nd Edition published by Wrox Press. Burdick has been named a Microsoft eMbedded MVP in 2001, 2002, 2003, and 2004.

Classes:

ETP-448 - Building Internet Applications with Microsoft's .NET Compact Framework

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John Canosa

Chief Scientist
Questra

John Canosa is CTO of Questra Corporation. His primary focus is on device communications and how companies can take advantage of pervasive device networking. He provides business and technology strategy based on experience with leading-edge technologies such as Web services, communications and embedded systems. Mr. Canosa has over 20 years of experience in both hardware and software design and has been a highly rated speaker at many industry events, as well as providing on-site seminars for Fortune 500 companies. John has a BSEE from Clarkson University and an MSEE from the Rochester Institute of Technology.

Classes:

- ETP-324 - Web Services in Embedded Systems
- ETP-402 - Fundamentals of Digital Imaging, Part 1
- ETP-422 - Fundamentals of Digital Imaging, Part 2



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Joe-Ming Cheng

Senior Engineer/Scientist

Hitachi Global Storage Technology

Joe-Ming Cheng is a member of performance analysis team at Hitachi Global Storage Technology and is a part-time associate professor at Silicon Valley University. He has worked at IBM Research and Development for 25 years on algorithm, SOC, storage system, embedded system, and design automation tool developments. He received an Outstanding Innovation Award and an Outstanding Achievement Award from IBM. Cheng has also worked on guidance system and air-borne CPU developments. Dr. Cheng holds an MS in (Biomedical Electronics) Scientific Instrumentation from UC Santa Barbara, and a PhD in Computer Engineering from UC Santa Cruz. He holds eight issued U.S. Patents.

Classes:

ETP-321 - AVR Microcontroller for Control Application Developments



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Carl Christensen

Staff Engineer
Thomson

Carl Christensen has been designing hardware and software for over 16 years. His projects include wired LAN equipment, driving simulators, fixed local loop wireless, digital video, forward error correction, power line LANs, and broadcast digital audio. Christensen has designed boards, drivers, application software, and ASICs. For the past few years, he has specialized in cutting edge FPGA design and system architectures for Thomson (brand names include RCA, Technicolor, and Grass Valley). His published work includes technical papers at the Synopsys User Group Meetings (SNUG), the National Association of Broadcasters (NAB) convention, and Xilinx Expert User Symposium (XEUS). Christensen has taught courses in HDL-based design and programming in industry and college settings. He currently has 16 patents/applications in review in the areas of forward error correction and broadcast routing systems. Christensen holds a BSEE from Utah State University as well as graduate level work in computer science.

Classes:

ETP-403 - The Perils of FPGA Timing Closure



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Embedded Systems Conference San Francisco

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Field Applications Engineer
Avnet Design Services

RC Cofer is a senior DSP design engineer for Soneticom with a BSEE from Florida Tech and a MSEE in communications and DSP from the University of Florida. His 15 years of embedded design experience include real-time DSP algorithm development, board design, debug and integration, transition to volume production, systems engineering, and embedded design project management. His technical focus is rapid system design and prototyping. Utilizing FPGAs in designs allows maximum flexibility while also reducing risk and schedule.

Classes:

ETP-309 - Designing with Soft Processor Cores in FPGAs, Part 1
ETP-329 - Designing with Soft Processor Cores in FPGAs, Part 2
ETP-343 - FPGA Design for Firmware Engineers, Part 1
ETP-363 - FPGA Design for Firmware Engineers, Part 2

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Niall Cooling

Director

Feabhas Limited

Niall Cooling has worked within the field of real-time embedded development for over 15 years. Having started his career working on defense systems, he moved to work for a major real-time operating system vendor. Since founding Feabhas in 1995, Cooling has furthered his experience of OO techniques for embedded systems. Cooling now lectures many Feabhas courses and has trained and offered UML, C, C++ and RTOS consultancy services to many major clients. Cooling is a Chartered Engineer (CEng) and a member of the BCS, IEEE and ACM.

Classes:

ETP-405 - C++: Inheritance, Interfaces and Thunks

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Robert Craig

Senior Software Developer
QNX Software Systems

Robert Craig is Senior Software Developer in the Kernel Group at QNX Software Systems Ltd. Mr. Craig has worked extensively in the Ottawa high technology industry in team lead and software architect roles with data communication companies and has over 12 years of experience in the embedded systems area. Mr. Craig holds a BSCS and a bachelors in physics from Memorial University of Newfoundland and a doctorate in physics from Heriot-Watt University in Edinburgh, Scotland where he worked on Optical Computing technologies.

Classes:

ETP-320 - Designing Applications for Symmetric Multi-Processing Systems



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Steven Dake

Senior Software Engineer
MontaVista Software

Steven Dake has been involved in open source Linux for over 10 years. He currently is a Carrier Grade software engineer for MontaVista software where he is a contributor to the startup team that engineered MontaVista Linux Carrier Grade Edition. Dake is an active member of the Open Source Development Lab Carrier Grade Linux technical working group where he develops with others the OSDL CGL specifications. He is also a contributor to the Service Availability Forum AIS working group where the AIS specifications are developed. For fun, he maintains an open source implementation of the Service Availability Forum's AIS specification accepting contributions from any interested parties. Steven received his BSCS from Northern Arizona University.

Classes:

ETP-304 - Implementing High Availability with the SA Forum Specifications



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James Darroch

Product Development Manager
Artesyn Communication Products

Jim Darroch is the Protocol Development Manager for Artesyn Communication Products. He has over 13 years experience working with networking protocols and systems, with hands-on experience of implementing X.25, ISDN, Frame Relay, SS7 and Sigtran. His exposure has ranged from a software engineer writing the code, to a senior engineer and team leader acting as software architect. Darroch holds a BSCS from Strathclyde University and lives in Edinburgh, Scotland.

Classes:

ETP-267 - Building Signaling Platforms with ATCA



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Don Davis

Senior Engineering Manager
Xilinx

Don Davis leads research and development of high-level tools at Xilinx. His current focus is on the compilation of complex algorithms described in standard software languages into high performance FPGA hardware implementation and hardware/software co-design. Davis has previously worked in the areas of reconfigurable computing, computer networks and satellite ground systems. His background includes hardware design (both FPGA and ASIC), software development and project management. He has seven patents covering areas as diverse as hardware architectures, communications/network processing, reconfigurable computing and high-level language tools. Davis received his BSEE from the University of Maryland in 1989 and recently earned an MBA from the University of Maryland.

Classes:

ETP-423 - Hardware/Software Codesign for Platform FPGAs



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Greg Davis
Engineering Manager, Compiler Development
Green Hills Software

Greg Davis is the technical lead of the compiler team at Green Hills Software, where he has been working for 10 years. His focus at Green Hills has been on optimization, code generation, and language issues. He graduated from the California Institute of Technology in 1995.

Classes:

ETP-364: Guidelines for Writing Portable Code



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Bruce Powel Douglass

Chief Evangelist
I-Logix

Bruce Powel Douglass has over 25 years' experience designing safety-critical real-time applications in a variety of hard real-time environments. He has authored ten books, including the Real-Time UML 3rd Edition: Advances in the UML for Real-Time Systems, Real-Time Design Patterns: Robust, Scalable Architectures for Real-Time Systems, and the definitive Doing Hard Time: Developing Real-Time Systems with UML, Objects, Frameworks, and Patterns. He worked with others on the UML 1 and 2 specifications and is a cochair for the Real-Time Analysis and Design Working Group in the OMG standards organization, focusing on the application of UML in real-time and embedded systems. Dr. Douglass is currently working on the Systems Modeling Language (SysML) specification. Dr. Douglass is the chief evangelist for I-Logix, an industry-leading vendor for model-based development tools, training, and consulting. Dr. Douglass has written ten books on software development and is on the advisory board for the Embedded Training Program. He speaks at many different academic and industry conferences but spends the majority of his time consulting to companies on development processes, process and project assessments, application of model-driven design, model-driven architecture, UML, real-time and safety critical systems design.

Classes:

ETP-221 - Effective Use Cases for Real-Time Systems

ETP-242 - SysML: The New Systems Modeling Language ETP-302 - DODAF and the UML

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Paul Ekas

Sr. DSP Marketing Manager
Altera Corporation

Paul Ekas joined Altera in August 2002 as the Senior DSP Marketing Manager in charge of the company's Code:DSP corporate marketing initiative. Ekas has more than 17 years of business experience in electronic design automation and complex semiconductor systems. Prior to joining Altera, Ekas was a director of product marketing at Morphics Technology where he was responsible for the 3G WCDMA infrastructure product line. Ekas has also held sales and engineering positions at Mentor Graphics, Silicon Designs, and Seattle Silicon. He holds a BSEE and MSEE from the University of Washington.

Classes:

ETP-460 - Complementing DSPs with FPGAs

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Bruce Emaus

President
Vector CANtech, Inc.

Bruce Emaus is president of Vector CANtech, a company that specializes in tools and embedded software components for distributed applications. With over 30 years of experience covering embedded software, hardware and systems, he is a leading expert in the area of distributed embedded systems. Mr. Emaus is also the chairman of SAE Embedded Software Standards Committee, an automotive electronics agenda that moves toward advancing the development of in-vehicle software. Bruce also ran his own electronics consulting company for over 20 years before joining Vector. As a University of Michigan graduate, Bruce's accomplishments include the development of Ford's first trip computer, Ford's first internally-created integrated circuit, the creation of Ford's first peer-to-peer UART-based protocol (ACP), and the development of a distributed electronic music system architecture before the advent of MIDI.

Classes:

ETP-340 - Introduction to Distributed Embedded Systems



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Tom Erkkinen

Embedded Applications Manager
The Mathworks

With more than eight years of embedded systems design experience, Tom Erkkinen specializes in embedded systems, spearheading an effort to foster industry adoption of automatic code generation for production released software. Before joining The MathWorks, Tom worked at Lockheed and developed control systems and software for programs including the Trident I & II missiles; Space Shuttle robotic manipulators systems; and Space Station robot HIL test Ia at NASA Johnson Space Center. Tom holds a BS degree in Aerospace Engineering from Boston University and a MSME from Santa Clara University.

Classes:

ETP-342 - Production Code Generation



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Jie Feng

Product Line Manager
Altera

Ms. Feng joined Altera, a programmable logic company, in 1999. Ms. Feng started as an Applications Engineer and later as a Technical Marketing Engineer for wireless market segment, and most recently as Product Line Manager for FPGA product marketing. Ms. Feng earned his masters degree from Stanford University in 2003 and bachelors degree from University of Toronto in 1999.

Classes:

ETP-262 - Leveraging Bit-Stream Encryption to Protect IP and Proprietary Designs



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Bryan Fletcher

Technical Program Manager
Memec

Bryan Fletcher holds BSEE & MSEE degrees from Utah State University. Fletcher has worked as a system's designer for both Hewlett Packard (Fort Collins, CO) and Evans & Sutherland (Salt Lake City, UT). While at HP, Fletcher worked on system development of HP's B- and C-class HPUX Workstations. At Evans & Sutherland, Fletcher was a hardware designer for E&S' first PC-based, PCI image generator. This image generator was the first of its kind to use an FPGA to perform all of the simulation image manipulation. Fletcher has worked for both Memec Insight and Avnet as a Gold-certified, Xilinx-dedicated Field Applications Engineer. Currently, Fletcher works for Memec's Technical Marketing Department. He is responsible for designing, testing, and supporting Memec's Spartan FPGA development board program as well as authoring and presenting Memec customer training material.

Classes:

ETP-367 - FPGA Embedded Processors: Revealing True System Performance



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Kim Fowler

Senior Engineer

Johns Hopkins Univ, Applied Physics Lab

Kim has over 20 years in designing and developing medical, military, and satellite equipment. He authored, *Electronic Instrument Design: Architecting for the Life Cycle*, published by Oxford University Press. He is Editor-In-Chief of the *IEEE Instrumentation & Measurement* magazine, writes the *Tried and True* column, and is an IEEE Distinguished Lecturer. He co-founded Stimsoft, a medical products company. He has published widely in engineering journals and has several patents.

Classes:

ETP-210 - Noise and Shielding

ETP-250 - Fantastic Failures

ETP-270 - Mission-Critical and Safety-Critical Development



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Lori Fraleigh

Director, Tools Technologies
Real-Time Innovations, Inc.

Lori Fraleigh is Director of RTI's ScopeTools product group where she is responsible for visualization and analysis tools for VxWorks and Linux. Lori has extensive experience designing and developing embedded debugging tools that focus on improving system performance and reliability with little overhead. Now a senior member of a small company, she has deep technical experience from her many hats, from customer support to technology evangelist. Lori leads seminars on debugging embedded systems in many venues. She holds an MSEE from Stanford and CEE from Purdue.

Classes:

[ETP-327 - The Ten Secrets of Debugging Embedded Systems](#)

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Steve Furr

Senior product manager
QNX Software Systems

Steve Furr is a senior product manager for QNX Software Systems and a coauthor of the Real-time Specification for Java (RTSJ). He currently serves as a technical member on several industry forums, including the Open Group's Real-time and Embedded Systems Forum, which is dedicated to expanding the marketplace for standardized real-time and embedded systems. In his 13+ years with QNX, Mr Furr has held various engineering positions, including software architect. He holds a BSCS.

Classes:

ETP-421 - Real-Time Programming in Java



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Zijad Galijasevic

Senior Embedded Software Engineer
The MathWorks, Inc

Zijad Galijasevic is a senior embedded software engineer at The MathWorks, Inc., Natick, MA. He received his PhD from Texas A&M University, College Station, TX in 2001. Dr. Galijasevic has been with The MathWorks since 2001 and is currently involved in the development of tools for model-based design and deployment.

Classes:

ETP-443 - Model-Based Design of Closed Loop Control for Embedded Systems Using Fixed Point Controllers



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Jack Ganssle

Chief Engineer
The Ganssle Group

Jack Ganssle writes for Embedded Systems Programming and has written four books on embedded systems and one on his sailing fiascos. He started developing embedded systems in the early '70s using the 8008. Since then, he's started and sold three electronics companies, including one of the bigger embedded tool businesses. He's developed or managed more than 100 embedded products, from deep sea navigational gear to the White House security system. Ganssle now gives seminars to companies worldwide about better ways to develop embedded systems.

Classes:

ETP-330 - Really Real-Time Systems
ETP-350 - Learning from Disaster

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Neil Gammage

Applications Engineer
Freescale Semiconductor

Neil Gammage is an Applications Engineer with Freescale Semiconductor. Mr. Gammage has extensive experience in real time computing in both architectural and software development roles with data communications companies in the Ottawa area. Mr. Gammage holds a BA degree in physics from Oxford University and has 40 years of experience in the computing, data communications, and semiconductor industries. He is currently working on devices for the embedded systems market.

Classes:

ETP-320: Designing Applications for Symmetric Multi-Processing Systems



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Nick Garnett

Chief Technical Officer
eCosCentric Ltd.

Nick Garnett is CTO of eCosCentric Ltd. He has 25 years experience in systems software, mostly in the embedded and real time domain. Garnett has worked on a wide variety of systems ranging from the Amiga operating system through highly parallel systems to virtual reality. Garnett designed eCos in 1997 while working for Cygnus Solutions and has continued to maintain and develop it since. Garnett holds a PhD in computing from the University of Cambridge, England.

Classes:

ETP-268 - An Introduction to eCos



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William Gatliff

Independent Consultant

Bill Gatliff is a freelance embedded developer and training consultant with 10 years of experience using GNU and other tools for building embedded systems targeting automotive, aerospace, and medical instrumentation applications. He is a contributing editor for Embedded Systems Programming, author of the Embedded GNU Jumpstart and Embedded Linux Jumpstart series of training materials, and a noted lecturer and widely quoted author on subjects related to embedded systems.

Classes:

ETP-206 - Implementing Downloadable Firmware with Flash Memory

ETP-245 - Embedded Linux Startup Code

ETP-265 - Embedded Linux Interrupt Code

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Rick Gentile

Senior DSP Applications Engineer
Analog Devices, Inc.

Rick Gentile leads the Blackfin DSP Applications Group at Analog Devices, Inc. Gentile has been widely published in domestic and foreign embedded processing trade magazines. Prior to joining Analog Devices, Rick was a member of the technical staff at MIT Lincoln Laboratory, where he designed several embedded DSP systems used in a wide range of radar sensors. He has also led several large software development teams for a variety of signal processing applications. He received a BS from the University of Massachusetts at Amherst and an MS from Northeastern University, both in electrical and computer engineering.

Classes:

ETP-362 - Programming Frameworks for Embedded Multimedia Applications



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Mark Gerhardt

Principal Architect
TimeSys Corporation

Mark Gerhardt is the Principal Architect at TimeSys Corporation. With 30 years experience designing and building real-time systems, he is a frequent lecturer on design methods, scheduling theory, and architecture development for time-critical systems. Schedulability tools and techniques, architecture design methods, and domain-specific architectures for high performance are Gerhardt's current focus of interest. His interests also include software and system engineering methods, system and software architecture and its relationship to programming languages.

Classes:

ETP-420 - Real-Time Architectures: Past, Present, and Future, Part 1
ETP-440 - Real-Time Architectures: Past, Present, and Future, Part 2



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Drew Gislason

President
San Juan Software

Drew Gislason has more than 18 years of experience in writing embedded systems software. He has written commercially available operating systems, a BIOS, device drivers, a GUI and networking software. Drew is now president of San Juan Software, a company that is focused on providing ZigBee software applications and custom engineering. He has authored articles for Dr. Dobb's Journal and other magazines and spoken at other conferences.

Classes:

ETP-449 - Application Development for ZigBee Wireless Networking



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Paul Gramann

Advisory Engineer IBM

Paul Gramann has over 20 years of experience in embedded systems development and support. In his 10 years with the IBM PowerPC Embedded Processors organization, he has assisted hundreds of customers with PowerPC software and hardware related issues. Gramann also authors and reviews technical documentation and develops and delivers technical training for IBM's application engineers and customers. Mr. Gramann has a BSEE from the University of Virginia and a MSCS from the University of Minnesota.

Classes:

ETP-466 - Introduction to the PowerPC Programming Model



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Todd Greenwalt

Director of Software Analysis
Metrowerks Corporation

Metrowerks Corporation's Todd Greenwalt serves as director of software analysis and manages the company's code analysis technology portfolios, including the CATS and CodeTEST product lines.

Mr. Greenwalt possesses more than 20 years experience in the embedded computing industry. Prior to joining Metrowerks in 2002, he served as general manager of embedded tools for Applied Microsystems Corporation. Mr. Greenwalt has also worked for several leading aerospace companies including Boeing and Olin Aerospace.

Classes:

ETP-470 - Safety Critical Software Verification: Lessons From the DO-178B Approach



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Steven Greffenius

Technical Publications Manager
Pathfinder Solutions, LLC

Since 1997, Steven has worked as a project manager and writer in the preparation of technical publications for both hardware and software systems. He has a PhD in social sciences from the University of Iowa, and his BA from Reed College.

Classes:

ETP-310 - How to Streamline Embedded Systems Development with Eclipse



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Michael Grischy

Software Consultant
Octave Software Group, Inc.

Mr. Michael Grischy has more than twenty years of experience in the software industry covering a broad array of applications, technologies, tools, and platforms. He has been a software consultant since 1992. His work has included many embedded systems projects in such diverse areas as network drivers, network protocols, printers, under-sea fluoroscopy, serial communications, payphone technology, and 802.11 wireless. Mr. Grischy owns his own consulting firm in partnership with David Simon who has written the popular book

Classes:

ETP-241 - Design Patterns for Tasks in Real-Time Systems

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Ben Harding

F AE

Avnet

Ben Harding is a Field Application Engineer for AVNET with a BSEE from the University of Alabama and extensive post-graduate and industry classes in Control Theory, DSP, and Parallel Processing. He has 13 years of embedded design experience including Real Time Embedded Operating Systems, design from concept through production, full life cycle management, and system engineering. He has extensive design experience with DSP and 8, 16 and 32-bit embedded processors and parallel processors.

Classes:

- ETP-309 - Designing with Soft Processor Cores in FPGAs, Part 1
- ETP-329 - Designing with Soft Processor Cores in FPGAs, Part 2
- ETP-343 - FPGA Design for Firmware Engineers, Part 1
- ETP-363 - FPGA Design for Firmware Engineers, Part 2



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David Haworth

Vertical Market Specialist - Embbd Apps
Tektronix

Classes:

ETP-208 - Debugging Elusive Digital Problems Quickly



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Charles Knutson

Asst Professor, Computer Science Dept
Brigham Young University

Charles Knutson is an assistant professor of computer science at Brigham Young University. He is the former vice president of R&D at Counterpoint Systems Foundry, and served as the chair of the test and interoperability committee of the Infrared Data Association (IrDA). His research interests include studying software engineering implications for embedded systems. Knutson holds a PhD in computer science from Oregon State University.

Classes:

ETP-209 - Short-Range Wireless Data Communications
ETP-360 - Verification and Validation for Embedded Software

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Jean Labrosse

President
Micrium, Inc.

Jean Labrosse is President of Micrium, Inc., a provider of high quality embedded software solutions. Mr. Labrosse is a regular speaker at the Embedded Training Programs and serves on the Advisory Board of the conference. Jean is the author of two books: MicroC/OS-II, The Real-Time Kernel and, Embedded Systems Building Blocks, Complete and Ready-to-Use Modules in C and has written numerous articles for magazines. He has an MSEE and has been designing embedded systems for many years.

Classes:

ETP-200 - Designing with Real-Time Kernels, Part 1
ETP-220 - Designing with Real-Time Kernels, Part 1
ETP-240 - Inside Real-Time Kernels, Part 1
ETP-260 - Inside Real-Time Kernels, Part 2



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Christian Legare

Vice President

Micrium

In his 22 years in the telecom industry, Christian Legare has taught classes and gave numerous presentations to customers. Christian was involved as an executive in large scale organizations as well as start-ups, mainly in Engineering and R&D. Christian is currently in charge of an IP (Internet Protocol) certification program at the International Institute of Telecom (IIT) in Montreal, Canada as their IP systems expert. The IIT is specialized in telecom training programs for operators and equipment manufacturers. Mr. Legare has a MSEE from the University of Sherbrooke, Quebec, Canada.

Classes:

ETP-308 - IP Version 6 and the Dual Stack



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Christopher Leidigh

Director of Embedded Communications
American Power Conversion

Christopher Leidigh has been programming in various languages for more than 14 years and has been doing embedded hardware and firmware design for eight years. Currently, he leads the embedded networking group at American Power Conversion, implementing SNMP and HTTP management platforms for power and environmental protection systems. Leidigh received a BS in bio-electrical engineering from Brown University.

Classes:

ETP-307 - Internet Messaging and Mail Protocols



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Doug Locke

Embedded Systems Consultant
Locke Consulting, LLC

Dr. Doug Locke is an independent consultant in real-time, embedded systems. He has spent more than 35 years intimately involved in the specification, architecture, design, and implementation of a wide range of real-time embedded systems. He is a frequent lecturer on systems and software architecture, distributed real-time systems, object oriented systems architecture, standards and real-time scheduling theory and practice, and was heavily involved in creating many real-time systems standards.

Classes:

ETP-420 - Real-Time Architectures: Past, Present, and Future, Part 1
ETP-440 - Real-Time Architectures: Past, Present, and Future, Part 2



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Tomasz Lukasiak

DSP Applications Engineer
Analog Devices

Tom Lukasiak is a DSP applications engineer at Analog Devices. He is currently focusing on Blackfin DSP products. He received a BSEE and an MSEE from Brown University.

Classes:

ETP-362 - Programming Frameworks for Embedded Multimedia Applications



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Sebastien Marineau-Mes

Senior OS Manager & Architect
QNX Software Systems

Sebastien Marineau-Mes is project leader for the Eclipse C/C++ Development Tools (CDT) project and a senior OS architect at QNX Software Systems. A popular speaker at embedded technology conferences, Mr. Marineau possesses a wide range of expertise, including real-time operating systems, protocol stacks, performance optimization, high availability architectures, and symmetric multiprocessing systems. Mr. Marineau spearheaded the development of the QNX Momentics development suite, an Eclipse-based graphical IDE, and currently heads the kernel group for the QNX Neutrino RTOS.

Classes:

ETP-320: Designing Applications for Symmetric Multi-Processing Systems



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Robert C. Martin

President
Object Mentor Inc.

Robert C. Martin has been a software professional since 1970. He is president of Object Mentor Inc., a team of experienced trainers, mentors, and consultants that serves its clients worldwide in the fields of OO, Patterns, UML, Agile Methodologies, and particularly eXtreme Programming. In 1995, Robert authored the best-selling book *Designing Object Oriented C++ Applications using the Booch Method*, published by Prentice Hall. In 1997, he was chief editor of the book *Pattern Languages of Program Design 3*, published by Addison Wesley. In 1999, he was the editor of *More C++ Gems*, published by Cambridge Press. He is also co-author, with James Newkirk, of *XP in Practice*, Addison Wesley, 2001. In 2002, he wrote the long awaited *Principles, Patterns, and Practices of Agile Software Development*, Prentice Hall, 2002. From 1996 to 1999, Robert was the editor-in-chief of the *C++ Report*.

Classes:

ETP-407 - Extreme Programming and Embedded Software Development



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Harpinder Matharu

Staff Engineer
IDT Inc.

Harpinder S. Matharu is a staff engineer for IDT Inc. Harpinder has more than 15 years of experience working as a software and hardware engineer in designing communication systems. His area of specialization is in the area of CPU architecture, coprocessors, peripherals, and the Interconnect. He has written several application notes and technical documents. He holds a degree in engineering and business.

Classes:

ETP-467 - Emerging Landscape of High Speed Serial Interconnect Standards



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Dale Mayes

Independent Consultant
Home Port Engineering LLC

Dale Mayes is a recognized industry leader, with 16 years of engineering and management expertise focused on software process creation, Internet enabling devices, and embedded software development. He has adapted DoD-2167A to small organizations with commercial vs. military timelines and budgets. Dale has presented papers at various appliance industry conferences. Currently, he is assisting an aerospace company on a DO-178b embedded software development project. Dale's degrees include in a BSCE, a BSEE, and an MBA.

Classes:

ETP-410 - Establishing Great Software Development Process(es) for Your Organization



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Stephen J. Mellor

Chief Scientist
Mentor Graphics Corp.

Stephen J. Mellor is an internationally recognized pioneer in creating effective, engineering approaches to software development. In 1985, he published the widely read Ward-Mellor trilogy Structured Development for Real-Time Systems, and in 1988, the first books defining object-oriented analysis. Stephen also published Executable UML: A Foundation for Model-Driven Architecture in 2002. His latest book MDA Distilled: Principles of Model-Driven Architecture was published in 2004. He is active in the Object Management Group, chairing the consortium that added executable actions to the UML, and he is now active in specifying MDA. He is a signatory to the Agile Manifesto. Stephen co-founded a company focused on tools to execute and translate UML models. He is now chief scientist of the Embedded Systems Division at Mentor Graphics. In his copious spare time, he chairs the IEEE Software Industrial Advisory Board. @Mentor.com

Classes:

ETP-261 - Executable UML

ETP-366 - Building and Implementing Concurrent Specifications

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Cyrylla Menon

General Manager
CAN in Automation (CiA)

Cyrylla Menon has been involved with data communication networks used in automation and automotive application for over 10 years. She is currently the general manager for CAN in Automation North America. Her responsibilities include training and consulting for industry personnel in automation and automotive networks, as well as marketing of CAN and other network products. She has been an active member of professional organizations such as SAE, ISO, IEEE, and ODVA, and holds a Masters in engineering and an MBA from the University of Michigan.

Classes:

ETP-370 - CANopen-Based Transducer Network
ETP-428 - Safety-Relevant Communication in Embedded Control Systems



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Larry Mittag

Lead Consultant
Mittag Enterprises

Larry Mittag has more than 25 years' design and development experience with embedded systems. He is one of the leading experts in the field of embedded systems, to include embedded Internet and wireless technologies, and is often invited to lecture and consult in the US and abroad. He is a regular class instructor for the Embedded Training Programs and regularly contributes to Embedded Systems Programming. Mittag holds a degree in physics and education from Wright State University.

Classes:

ETP-229 - Wireless Protocol Stacks
ETP-249 - Understanding and Using the 802.11 Standards
ETP-269 - 802.11 Security



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Arefeen Mohommad

Motor Control Engineer
Texas Instruments

Arefeen Mohommad is a system application engineer at Texas Instruments Inc., Houston, TX. He received his PhD from Texas A&M University, College Station, Texas in 1994. Dr. Arefeen joined Texas Instruments, in 1995 and currently working in the area of embedded control systems.

Classes:

ETP-443 - Model-Based Design of Closed Loop Control for Embedded Systems Using Fixed Point Controllers



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Rajat Moona

Professor
IIT Kanpur

Rajat has been teaching at IIT Kanpur for the past 13 years. His research interests include operating systems, embedded systems, architecture, VLSI design. He has worked with several companies as consultant on helping them develop methods for improving the design of the systems. He has worked extensively for characterising the performance of the processors and embedded systems through his research. He has also published several papers in this area.

Classes:

ETP-441 - Measuring and Tuning Real-Time Performance of Embedded Systems

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Gordon Mortensen

Engineering Director, Portable Power Group
National Semiconductor Corporation

Gordon Mortensen is engineering director of Advanced Technology for the Portable Power Group at National Semiconductor Corporation. Mortensen has 22 years of experience in the semiconductor industry in engineering management, as a design engineer and as a product engineer. Experience includes developing 4-bit, 8-bit and 16-bit micro-controller products, x86 platform chipsets and PowerWise(TM) portable power management products created to extend battery life in portable devices. He received a BSEE from the University of Utah, has three patents pending and holds three U.S. patents assigned to National Semiconductor.

Classes:

ETP-444 - Power Management Strategies in Embedded Applications,
Part 1
ETP-464 - Power Management Strategies in Embedded Applications,
Part 2



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Niall Murphy

Consultant
Panelsoft Ltd.

Niall Murphy has been writing software for user interfaces and medical systems for 12 years. He is the author of "Front Panel: Designing Software for Embedded User Interfaces." He provides training and consulting on user interface issues and he writes the Murphy's Law column for Embedded Systems Programming magazine.

Classes:

ETP-230 - Top Ten Usability Mistakes
ETP-246 - Memory Management, Part 1
ETP-266 - Memory Management, Part 2



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Kelvin Nilsen

Chief Technology Officer
Aonix

Kelvin Nilsen joined the Computer Science faculty at Iowa State University in 1988. There, his pioneering research in real-time programming resulted in five commercial patents. Dr. Nilsen's seminal research on the topic of real-time Java led to the founding of NewMonics. In 2003, Aonix acquired NewMonics. Today, Dr. Nilsen serves as CTO of Aonix. In this role, he oversees the complete family of Aonix products providing life-cycle support for development of safety-critical and mission-critical systems. Dr. Kelvin Nilsen earned his degree in physics from Brigham Young University and his MSCS and PhD from the University of Arizona.

Classes:

ETP-425 - High Assurance Java for Mission-Critical Systems, Part 1
ETP-445 - High Assurance Java for Mission-Critical Systems, Part 2



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Ryuji Okamura

Development of Road Vehicle
Toyota Motor Corporation

Ryuji Okamura is an engineer for the electronics engineering division of Toyota Motor Corporation. Since 2000, Okamura has been engaged in development of embedded software and its environments for automotive systems, which are engine control, electronic fuel injection and so on. Okamura's responsibility is to design embedded software for researching a new control systems and to provide the new methods for design of these systems. Okamura holds an MSEE from Nagoya University, Japan.

Classes:

ETP-450 - The Hardware/Software Co-design for Road Vehicle Control System

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Robert Oshana

Engineering Manager, DSP
Texas Instruments

Rob Oshana has been actively involved in the real-time embedded space for over 22 years. He currently manages a software development tools group for embedded DSP and microcontroller development. Rob speaks annually at conferences and recently earned the Embedded Systems 5 year teaching award. He teaches graduate courses at Southern Methodist University and National Technological University in the areas of Embedded Systems, and several other Software Engineering courses. He has over 40 publications in the area of Software Engineering and Embedded Systems

Classes:

- ETP-243 - Embedded Systems Programming Using DSPs
- ETP-322 - Understanding Compilers and Optimizations for Embedded Systems
- ETP-368 - Power Optimization Techniques for Embedded Systems Programmers



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Ali Paasimaa

Architect, Sales, Engineering and Consulting
Solid Information Technology

Ali Paasimaa currently holds the position of architect, sales engineering and consulting at Solid Information Technology. For the last four years Paasimaa's work has mainly focused around pre-sales, customer training, consulting projects, and conducting design & implementation workshops on distributed and highly available transactional data management. Prior to joining Solid in 2000 he gained experience at Fujitsu Services and Bowne & Co. He has spoken at conferences and is the author of several articles on embedded and distributed data management. Paasimaa holds BSCS from the University of Helsinki, Finland, with a minor in Industrial Management from the Helsinki University of Technology.

Classes:

ETP-446 - Data Management for Highly Available Embedded Systems

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Olaf Pfeiffer

President

Embedded Systems Academy

Olaf Pfeiffer worked for several years as technical support manager for an embedded systems development tools company. Pfeiffer is one of the founders of the Embedded Systems Academy and represents the CiA (CAN in Automation users and manufacturers group) in the USA. His expertise covers topics such as how to shorten the time-to-market of embedded systems engineering projects and a variety of embedded networking technologies, including CAN, CANopen and embedded internetworking. Pfeiffer earned his degree from the Technical Computer Science at the Co-Op University Karlsruhe, Germany. ETP-447 - Covering Multiple Embedded Networking Technologies with CANopen

Classes:

[ETP-468 - Bridging Embedded Network Technologies](#)

[ETP-447 Covering Multiple Embedded Networking Technologies with CANopen](#)



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John Pocs

Senior System Application Engineer
NEC Electronics America

John Pocs, senior application engineer, has been with NEC Electronics America's microcontroller group for seven years, supporting customer applications and development tools for 32-bit microcontrollers. He has more than 20 years of experience in the semiconductor industry. He received a Diploma Engineer degree in Industrial Electronics from Polytechnic Institute of Iasi, Romania and an MSEE from San Francisco State University. Pocs has extensive experience training FAEs, as well as presenting at national sales and training conferences.

Classes:

ETP-462 - MCUs for Motor Control

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Robert Poor

Chief Technology Officer
Ember Corporation

Robert Poor is a recognized authority on wireless embedded networking. He founded Ember in 2001 based on his research at MIT, pioneering a new class of wireless network based on inexpensive, scalable, easily-deployed devices that can do anything from controlling a building's lighting and climate to keeping truckloads of fish from spoiling. His patented networking intelligence stack is the heart of Ember's embedded radio frequency (RF) mesh networking technology. He holds a Bachelor of Fine Arts degree from Oberlin Conservatory, a Masters degree and a PhD from MIT. He is an active member of the IEEE and serves on its 802.15.4 wireless standards task force. He is a founder of the Wireless Industrial Network Alliance (WINA), a coalition of 40 companies promoting industrial wireless applications. Poor is an unrepentant musician, photographer and philanthropist with a passion for developing educational programs in developing countries.

Classes:

ETP-323 - Wireless Embedded Networks: Connectivity for Everyday Objects



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Murugavel Raju

MSP430 Applications Manager
Texas Instruments

Murugavel Raju currently works as the MSP430 World wide Applications Manager for Texas Instruments, Dallas. He was the Worldwide winner of the TI analog design challenge 1999 and was awarded \$40000 grand prize. He was also one of the winners of the Motorola Discover an Inventor MCU design contest 1998 held in India.

Classes:

ETP-203 - Programmable Embedded Peripherals Simplify Complex Tasks



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Ugo Ruggeri

Technical Manager
Upix elettronica s.a.s.

Ugo Ruggeri is technical director at Upix elettronica s.a.s., an italian electronic design company. He has been involved in embedded system design since 1989. He did work in vehicle gas exhaust analysis systems. He graduated cum laude in Electronic Engineering from the University of Bologna, Italy.

Classes:

ETP-347 - Slow Process Control: A Modeling/Simulation Approach



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Peter Ryser

Mgr Embedded SW Systems Eng
Xilinx

Classes:

ETP-442 - Software Defined Radio with Reconfigurable Hardware and Software



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Dan Saks

President

Saks & Associates

Dan Saks is the President of Saks & Associates, a training and consulting company specializing in C++. He is a contributing editor for Embedded Systems Programming and a member of the advisory board for The C/C++ Users Journal. He has also written columns for The C++ Report, Software Development magazine and the Windows Developer's Journal. Dan is co-author of C++ Programming Guidelines and co-developer of Suite++: The Plum Hall Validation Suite for C++. He served for many years as secretary of the ANSI and ISO C++ standards committee, and continues to follow the committees' activities.

Classes:

ETP-305 - C and C++ Gotchas, Part 1

ETP-325 - C and C++ Gotchas, Part 2

ETP-345 - Representing and Manipulating Hardware in Standard C and C++

ETP-365 - Writing ISRs in C++

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Miro Samek

President
Quantum Leaps

Miro Samek is the president of Quantum Leaps, a provider of real-time, state machine-based application frameworks for embedded systems. He is the author of "Practical Statecharts in C/C++" (CMP Books, 2002), has written numerous articles for magazines, and is a regular speaker at the Embedded Training Program. Before founding Quantum Leaps, Miro worked as Software Architect at Global Locate (San Jose, CA), where he designed GPS software for mobile phones and before that he designed GPS receiver software for IntegriNautics Corporation (now Novariant, Menlo Park, CA). Miro started his embedded career at GE Medical Systems, where he has developed safety-critical, real-time software for diagnostic imaging x-ray machines. He earned his PhD in nuclear physics at GSI (Darmstadt, Germany).

Classes:

ETP-406 - Practical Statecharts for Embedded Systems, Part 1
ETP-426 - Practical Statecharts for Embedded Systems, Part 2

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Ram Sathappan

Biometrics Solutions Manager
Texas Instruments

Ram Sathappan serves as the manager in charge of developing and promoting TI DSP based solutions for the biometrics industry. Since the DSP Emerging End Equipments group started up in 2001, Sathappan has been involved in evolving a business strategy for biometrics, developing the business for TI by setting up of the right infrastructure and product marketing for the addition of new customers. During his seven-year tenure at TI, Sathappan worked as a Design Engineer with the Microcontrollers group and was the design team lead from 1997 to 1999. In 2000, he became involved with the Microcontroller marketing group. In 2001, when the DSP Emerging End Equipments group started, he joined as the leading Biometrics manager. Sathappan attained a Bachelor of Engineering in Electronics Engineering from Manipal Institute of Technology, India followed by a MSCE from Syracuse University. He then received his MBA in marketing while at TI at the University of Texas in Austin.

Classes:

ETP-341 - Case Example: Implementing DSPs in Biometric Systems

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Ted Schleich

Sr. Systems Software Engineer
Universal Avionics Systems Corporation

Ted Schleich is currently an embedded software engineer at Universal Avionics Systems Corporation in Tucson, Arizona and a software engineering graduate student at the University of Texas at Austin. He has a broad background that includes degrees in data processing, electronics engineering, and business administration with experience in development, field service, and manufacturing.

Classes:

ETP-306 - Optimizing C for Embedded Systems

ETP-328 - Networking Technologies for Low-Level Embedded Systems



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Kevin Schutz

Product Manager
Atmel Corp

Kevin Schutz joined Atmel in 1989, has over 20 years experience in the semiconductor industry, and is currently the product manager for Secure Products within the North American ASIC and ASSP business unit. He is a key member of the team at Atmel developing products in support of the Trusted Computing Group. Prior to joining Atmel, Mr. Schutz worked for a number of high tech companies including Mostek and Honeywell. He has worked in a variety of areas, including the design of custom mixed-signal products, embedded processors and secure cryptographic processors. Mr. Schutz received his BSEE from Colorado State University, and both a MSEE and an MBA with a focus in technology development from the University of Colorado.

Classes:

ETP-429 - Integrating the Trusted Platform Module into Embedded Systems



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Vitaliy Slobotskoy

Software Engineer
Empirix Corporation

Vitaliy Slobotskoy is a software engineer at Empirix Corporation. Most recently he was a senior software engineer at Freescale Semiconductor Corporation, where he was involved in network processor application design, benchmarking and microprocessor modeling. Mr. Slobotskoy has 9 years of embedded systems development. He holds an MSCS from Northeastern University, and BS in Applied Mathematics from the St. Petersburg IFMO, Russia.

Classes:

ETP-344 - Real-Time Application Profiling for Improved Processor Utilization

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Matthew Sottek

Software Platform Engineer
Intel

Matthew Sottek is currently a lead developer in the Intel embedded graphics device driver development team. In this project, he is involved from the architectural work down to the actual implementation, which involves a general reusable graphics device driver framework that has been adapted to Windows 2000, XP, CE and Linux XFree86. In addition, Sottek was involved in porting existing monolithic device driver to the new framework.

Classes:

ETP-461 - Scalable and Platform Agnostic Device Driver Architecture



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Timothy Stapko

Software Engineer
Z-World, Inc./Rabbit Semiconductor

Timothy Stapko is a software engineer at Z-World, Inc and Rabbit Semiconductor. For over three years he has worked on Dynamic C, Z-World's proprietary C-based language for the Rabbit processor. Recently, Stapko was the lead developer of a Secure Sockets Layer (SSL) implementation in Dynamic C for the Rabbit. Tim holds a MSCS from the University of California, Davis.

Classes:

ETP-348 - Embedding SSL: Internet Security for 8-bit Systems



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Dave Stewart

Chief Technology Officer
Embedded Research Solutions, INC.

Dave Stewart is the executive VP and CTO of Embedded Research Solutions, LLC. His research areas include real-time operating systems, miniature software for pervasive computing, device driver methodology, hardware-software co-design, component-based software technology, automated analysis, and debugging tools. Stewart earned his PhD in computer engineering from Carnegie Mellon University.

Classes:

ETP-204 - Measuring Execution Time and Real-Time Performance, Part 1
ETP-224 - Measuring Execution Time and Real-Time Performance, Part 2
ETP-244 - The 25 Most Common Mistakes with Real-Time Software Development, Part 1
ETP-264 - The 25 Most Common Mistakes with Real-Time Software Development, Part 2
ETP-349 - Pervasive Computing Applications and Wireless Sensor Networks



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Gary Stringham

System/Software Engineer Specialist
Hewlett-Packard Co.

Gary Stringham has been with Hewlett-Packard Co. for 21 years with the last 13 years being in firmware design for HP LaserJet printers. He has established device driver standards and has influenced many design changes in custom ASICs. Gary has been awarded five patents and has over 20 pending. He is writing a book, "Firmware-friendly Chip Design Practices." He is a frequent and popular speaker. Gary holds a BSEE from Brigham Young University and an MSEE from Utah State University.

Classes:

ETP-207 - RTL Design Practices that Will Improve Firmware Development

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Arun Subbarao

Director, Technology & Product Development
LynuxWorks

Arun Subbarao is the director of technology & product development at LynuxWorks. Arun has extensive experience in the embedded software industry working on Unix, Linux & RTOS kernels, networking protocols and high availability. Arun has been a panelist at conferences and has authored white papers & articles for trade journals. He has also taught several classes in embedded software design at LynuxWorks. Arun holds a CS from India, MSCS from SUNY Albany and MBA from Santa Clara University.

Classes:

ETP-300 - Secure Embedded OS: A Technology Overview



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Tracy Thomas

Engineering Manager
eSOL, Inc.

Tracy Thomas is the engineering manager at eSOL, Inc. She manages the local engineering team and their projects and coordinates with the engineering team at eSOL Co., Ltd. in Tokyo. Tracy has embedded systems software development experience and expertise, especially in embedded networking. She formerly worked at U.S. Software as a project manager and software engineer. Tracy holds a PhD in Physics from Northwestern University.

Classes:

ETP-400 - Multiprocessing in Embedded Systems



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Raetta Towers

Lead Software Engineer
EmbeddedPlus Engineering

Raetta Towers is a lead software engineer at EmbeddedPlus Engineering and currently assists organizations transitioning to new technologies like UML and Model Driven Architecture (MDA). She provides UML training support to the Defense and Aerospace industries and is currently a UML instructor for the Army's Future Combat Systems (FCS) program. She is considered an expert in the application of object-oriented design principles utilizing UML and SysML to improve both business and engineering processes. Towers also has significant experience with next generation application development including communication software, scheduling software, and error-detection software suites.

Classes:

ETP-326 - Modeling and Simulation Using UML, Part 1
ETP-346 - Modeling and Simulation Using UML, Part 2



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Mike Trimborn

LabVIEW FPGA Product Manager
National Instruments

Mike Trimborn is a LabVIEW FPGA and DSP Product Manager at National Instruments. He earned a BS in mechanical engineering from the University of Texas at Austin. While at National Instruments, Mike has also served as Product Manager for LabVIEW Real-Time and as an Applications Engineer for working on specific implementations using LabVIEW to test embedded devices.

Classes:

ETP-463 - Integrating DSP Design and Test for Rapid Product Development



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Joe Tykowski

Software Engineer
AuthenTec

Joe Tykowski has 20 years experience making embedded systems software and hardware that works Tykowski holds a BSEE from Stevens Institute of Technology.

Classes:

ETP-301 - Writing Your First WinCE USB Device Driver



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Mark Vanfleet

Senior INFOSEC System Security Analyst
National Security Agency

Classes:

ETP-465 - Secure Safety-Critical Distributed Embedded Systems



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Thomas Herbert

VP Technology
Infosecure Open Systems

Tom Herbert is a frequent speaker at ESC and has published several articles in Embedded Systems Programming. He is currently publishing the book, "The Linux TCP/IP Stack: Networking For Embedded Systems." Recently he worked on an IP router for Joint Tactical Radio System at Innovative Concepts Inc. Previously, he worked for Wind River, and before that at Divx, a startup in DVD copy protection. Long ago, he was at Xerox Corporation and Eastman Kodak Company where he helped design and build on networked printers, scanners and computer vision projects. He holds a patent in pattern recognition. He received his BS from Binghamton University.

Classes:

ETP-223 - TCP/IP for Embedded Engineers

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Joseph Jacob

Sr. Vice President

Objective Interface Systems, Inc

Joseph Jacob is Senior Vice President of Objective Interface Systems, Inc, where his responsibilities include leading the product management team. Objective Interface is leading the MILS middleware initiative to secure the communications between safety-critical and security-critical systems with EAL-7 COTS software. The MILS middleware team includes Objective Interface, National Security Agency, U.S. Air Force Research Laboratory and Lockheed Martin. Joe has a BA from the University of Illinois at Urbana-Champaign with a double major in economics and political science, and his JD degree from the Harvard Law School.

Classes:

[ETP-465 - Secure Safety-Critical Distributed Embedded Systems](#)



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Ton Janssen

Software Engineer
Oce Technologies BV

Janssen studied "computer technics" in Venlo until 1984. He started writing test software for CT and later system software for MR medical System at Philips. Janssen moved to Oce Technologies in 1998 where he now focuses on Real time embedded SW development using a model driven approach.

Classes:

ETP-401 - Model Driven Development of Resource Constrained Embedded Applications



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David Kalinsky

Director of Customer Education
OSE Systems

David Kalinsky is director of customer education at OSE Systems. He is a popular lecturer and seminar leader on technologies for embedded software in North America and Europe. In recent years, he has built high-tech training programs for a number of Silicon Valley companies, on aspects of software engineering for the development of real-time and embedded systems. Before that, he was involved in the design of many embedded medical and aerospace systems. Kalinsky holds a PhD in nuclear physics from Yale.

Classes:

ETP-202 - Principles of High Availability Embedded Systems Design, Part 1

ETP-222 - Principles of High Availability Embedded Systems Design, Part 2



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David Katz

Senior DSP Applications Engineer
Analog Devices, Inc.

David Katz is a senior applications engineer at Analog Devices, Inc., where he is involved in specifying and supporting Blackfin media processors. He has published dozens of embedded processor articles both domestically and internationally. Previously, he worked at Motorola, Inc., as a Senior Design Engineer in cable modem and automation groups. David holds both a BSEE and a MSEE from Cornell University.

Classes:

ETP-362 - Programming Frameworks for Embedded Multimedia Applications



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Christian Keydel

Director of Applications
Embedded Systems Academy

Christian Keydel has been involved with the various aspects of embedded hardware and software design since 1994, starting his career as an R&D engineer for In-circuit Emulators. As a director and tutor of the Embedded Systems Academy, Christian supervises new class development and teaches and consults clients on embedded technologies including CAN and CANopen, Embedded Internetworking, Real-Time Operating Systems, and several microcontroller architectures as well as the associated development tools. He is a frequent speaker at the Embedded Training Programs and the Real-Time and Embedded Computing Shows and co-authored the book "Embedded Networking with CAN and CANopen" by Annabooks/RTC Group. Keydel holds a and MSEE and a MSCS from the University of Karlsruhe, Germany.

Classes:

ETP-447 - Covering Multiple Embedded Networking Technologies with CANopen



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Russell Klein

Engineer

Mentor Graphics Corporation

Russell Klein is an engineer with Mentor Graphics and is one of the original developers of the Seamless hardware/software co-verification environment. He holds three patents in the area of hardware/software co-verification and has published numerous articles on the subject. Klein has over 20 years of technical experience in system verification working at various electronic design automation companies.

Classes:

ETP-441 - Measuring and Tuning Real-Time Performance of Embedded Systems



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Paul Knot

Software Manager
4RF Communications Ltd

Paul Knot currently leads a team of software developers at a private company developing world-class digital microwave radio products. He has been working in the field of embedded product development for over 20 years, and has held positions ranging from software designer to embedded systems technology leader with numerous companies. After graduating from the University of Witwatersrand in Johannesburg with a BSEE, he returned to do post graduate study and learn more about software engineering. During the course of his working career, he has written embedded software for aircraft navigation systems, enhanced software for a missile tracking system, developed telco interfaces for trunked radio systems, and managed various embedded hardware and software development projects.

Classes:

ETP-404 - Selecting Linux as an Embedded Operating System



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Albert Wang

CTO

Stretch Inc.

Albert Wang is co-founder and CTO of Stretch. Previously, Wang was chief engineer at Tensilica, where he invented the TIE language and developed the TIE compiler. Prior to that, he was part of Synopsys' advanced technology group and developed key algorithms for timing-driven logic optimization and fast static timing verification for Design Compiler. Wang earned BSCE and applied mathematics from UC San Diego, as well as his PhD in electrical engineering and computer science from UC Berkeley.

Classes:

ETP-409 - Hardware As Software: Designing with Configurable Processors



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Tim Wescott

Owner

Wescott Design Services

Tim Wescott is an electrical engineer and owner of Wescott Design Services, an embedded systems design company. He has been closing embedded control loops in software for over 10 years.

Classes:

ETP-227 - Basic Control Theory for the Software Engineer

ETP-247 - PID without a PhD



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Jason Wilson

Senior Software Engineer
Pathfinder Solutions, LLC

Jason Wilson applies software engineering principles to model automation and transformation. He develops tools for model transformation, and applies these tools to embedded systems. Java mappings are a special focus of his work. Mr. Wilson has his BSCS from Worcester Polytechnic Institute, and is pursuing an MSCS in automated verification as well. When not engaged in the development of new software engineering tools, he conducts classes of his own and contributes much to the many groups he participates in.

Classes:

ETP-310 - How to Streamline Embedded Systems Development with Eclipse

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Joe Wlad

Product Manager, Aerospace & Defense
Wind River Systems

Joe Wlad is a product manager for Wind River in Alameda, CA and is responsible for all safety-critical products in the industrial, medical and aerospace markets. Mr. Wlad has over 19 years of safety-critical systems design, development, test and evaluation experience, including work at Intermetrics, Inc., McDonnell-Douglas Aircraft Company in the MD-11 Test and Certification organization and United Airlines' B747 Fleet engineering and modification organization. Mr. Wlad has also worked for Trimble Navigation as an engineering manager in development and FAA approval of military GPS sensors. He is an FAA DER for Systems and Equipment and Software, is an active private pilot and has co-authored three patents on Global Positioning System integrity functions. Joe Wlad holds a BS in aerospace engineering from the University of Buffalo and a MBA from Santa Clara University.

Classes:

ETP-408 - Meeting RTCA/DO-178B/12B and ARINC 653 Safety Requirements for Critical Systems



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Axel Wolf

Applications Manager
Philips Semiconductors

Axel Wolf manages the Philips Microcontroller Product Support Group in Sunnyvale, CA. He gained more than seven years of experience on CAN and microcontroller-based applications in his previous positions as Director of Classes at Embedded Systems Academy, Product Applications Manager at Infineon Technologies and Application Specialist at Siemens Semiconductors. Wolf organized similar successful CAN tutorials at almost every Embedded Training Program since ESC West 1997. He holds an BSEE from the University of Cooperative Education in Stuttgart, Germany.

Classes:

ETP-468 - Bridging Embedded Network Technologies

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Dale Word

Assistant Professor
California State University, Chico

Dale Word is an assistant professor in the Electrical and Computer Engineering Department at California State University, Chico. After spending over 15 years as an Embedded Developer, Manager and Consultant, he recently joined the faculty at CSU Chico to focus on teaching topics related to Embedded Systems Design and Development. His background includes extensive work in Embedded Networking, Equipment Control, and Servo Control Systems. Word holds a BSCS from UC San Diego, and an MSCS from CSU, Chico.

Classes:

ETP-430 - A Skills List for Developing Embedded Software

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Darcy Wronkiewicz

Director of Product Management
Green Hills Software

Darcy Wronkiewicz has been working in the embedded software industry since 1996 where she has held positions in software development and product design. Currently, Darcy is the Director of Product Management at Green Hills Software where she provides direction for the development of next generation tools and methods to enable the creation of successful embedded products. Darcy holds a BS in Computer Science from the University of California, Santa Barbara.

Classes:

ETP-427 - Debugging Embedded Linux Systems



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Bob Zeidman

President
Zeidman Consulting

Bob Zeidman is the President of Zeidman Technologies, a vendor of tools for embedded systems hardware and software development. Bob has designed ASICs, FPGAs, and PC boards for RISC-based parallel processor systems, laser printers, network switches and routers, and other systems for clients including Apple Computer, Cisco Systems, Intel, and Texas Instruments. He has written papers on hardware and software design methods, and has taught courses at conferences throughout the world. He is the author of the textbooks Verilog Designer's Library, Introduction to Verilog, and Designing with FPGAs and CPLDs. Bob was the recipient of the 1994 Wyle/EE Times American By Design Award and other engineering, writing, and scholastic awards. Bob holds a patent in software synthesis, an MSEE from Stanford University, as well as a BSEE and a BSP from Cornell University.

Classes:

Bob Zeidman is teaching a full-day tutorial, which is not included on this CD.



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ETP-200 Designing with Real-Time Kernels, Part 1

Level: Intermediate

Does your next embedded system need a real-time kernel (also known as an RTOS)? This class examines the costs associated with an RTOS, whether you can actually use one, how to set task priorities, how to use some of the most common services provided by a kernel, how some can reduce priority inversions, and more. This class uses a combination of code, graphics, animations, and running examples on an actual target CPU to show you what a kernel can do. This is the first class in a two-part series.

What You'll Learn: Whether you can use a kernel in your embedded system and how to use some of the most common services provided by commercial kernels.

Prerequisites: Knowledge of C Programming required.

Target Audience: Anyone who wants to determine whether a real-time kernel is needed and need to know how to select a commercial kernel.

With: Jean Labrosse

Tuesday, 8 March 2005

8:30am - 10:00am



[View the paper.](#)



[See the slides.](#)

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ETP-201 Linux 101

Level: Introductory

A large number of engineers grew up in the embedded world writing assembly language or C programs without reference to an operating system. Today Linux, a "free" operating system with full source code, looms large on the embedded horizon. Protected mode memory, the root filesystem, the Unix process model, device drivers--these are just some of the issues covered to give embedded engineers the tools they need to understand Linux and to use it effectively.

What You'll Learn: Insight into what Linux is, how it fits into the embedded space, and why you should care.

Prerequisites: Fluency in C and basic computer architecture knowledge required.

Target Audience: This class is aimed at engineers, like myself, who may have started out doing hardware design and now find themselves confronting software issues that seem far too abstract. They've done some programming, they understand C and they may even have interfaced to a real-time operating system. Now they're forced to confront more advanced operating system issues as they compete in the "all important" time-to-market race.

With: Doug Abbott

Tuesday, 8 March 2005
8:30am - 10:00am



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ETP-202 Principles of High Availability Embedded Systems Design, Part 1

Level: Introductory

High availability systems design is based on a combination of redundant hardware components and software to manage fault detection and correction. This must be done without human intervention to achieve "five-nines" (99.999%) or greater availability, equivalent to less than 1 second of downtime per day. This class discusses basic hardware N-plexing and voting issues, as well as software and system fault tolerance techniques appropriate for embedded systems, starting with the static method of N-version programming. A number of dynamic software/system fault tolerance techniques are surveyed and the class ends with a forward error recovery technique. This is the first class in a two-part series.

What You'll Learn: How to design embedded systems, including hardware and software, that are required to continue providing service despite the occurrence of internal and external faults.

Target Audience: Embedded system and software designers who design and develop hardware and software for embedded systems that are required to continue providing service despite the occurrence of internal and external faults.

With: David Kalinsky

Tuesday, 8 March 2005
8:30am - 10:00am



[View the paper.](#)



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ETP-203 Programmable Embedded Peripherals Simplify Complex Tasks

Level: Intermediate

Today's measurement world requires complex measurements that smart peripherals can't accommodate. One solution is programmable peripherals. CPLDs are one alternative but another approach is to have another set of CPU and memory attached to the smart peripheral. Changing the embedded software of the peripheral changes its function. This class describes this approach, and describes an electricity energy measurement meter as an application that can benefit from the approach.

What You'll Learn: How a second processor can handle complex tasks in low-power embedded applications, leaving less intensive functions to the main processor.

Target Audience: Designers of ultra low power industrial embedded systems, AC parameter measurement designers, General Microcontroller developers, Electricity meter manufacturers, General Metering manufacturers and developers that use high performance analog interface in their embedded applications.

With: Murugavel Raju

Tuesday, 8 March 2005
8:30am - 10:00am



[View the paper.](#)



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ETP-204 Measuring Execution Time and Real-Time Performance, Part 1

Level: Intermediate

Many embedded systems require hard or soft real-time execution. This class presents a variety of techniques, at both coarse-grain and fine-grain levels, to measure the execution time of both user code and operating system overhead. The measurements can then be used as the basis for accurate real-time scheduling analysis, for identifying timing problems, or to know what code needs to be optimized. This is the first class in a two-part series.

What You'll Learn: Techniques for measuring the real execution time of embedded programs, including advantages and disadvantages.

Prerequisites: Knowledge of C or C++ and basic operating system concepts required.

Target Audience: Programmers and software engineers building code, who need to ensure that real-time constraints are met or maximize the use of limited processing power.

With: Dave Stewart

Tuesday, 8 March 2005

8:30am - 10:00am



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ETP-205 Embedded Programming 101, Part 1

Level: Introductory

This class covers a number of key concepts associated specifically with real-time embedded programming. Core topics include writing reentrant code, using the volatile keyword, and interacting with peripheral control and status registers through memory-mapped I/O. In addition, issues such as interrupt latency, watchdog timers, endianness, and determinism will be discussed. The class also uncovers subtle features of the firmware development process, including C startup code, cross-compilation, relocation, and remote debugging. This is the first class in a two-part series.

What You'll Learn: How to write software that interfaces directly to hardware, including how to handle interrupts and access peripheral control and status registers through pointers, structures, and bitfields.

Prerequisites: Familiarity with C required.

Target Audience: Programmers who have limited experience writing real-time embedded software or device drivers, and other folks working close to the hardware/software interface for the first time.

With: Michael Barr

Tuesday, 8 March 2005
8:30am - 10:00am



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ETP-206 Implementing Downloadable Firmware with Flash Memory

Level: Intermediate

This class presents several approaches to implementing field reprogrammability in embedded systems that use flash memory. The discussion includes source code, descriptions of the imitations and advantages of each approach, and ways to avoid common mistakes associated with downloadable firmware capabilities.

What You'll Learn: A microprogrammer-based approach to flash memory reprogramming, and how this provides for safe and flexible field updates of embedded firmware.

Prerequisites: C Programming Experience required.

Target Audience: Embedded developers who want a safe and flexible capability to upgrade embedded firmware in the field.

With: William Gatliff

Tuesday, 8 March 2005
8:30am - 10:00am



[View the paper.](#)



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ETP-207 RTL Design Practices that Will Improve Firmware Development

Level: Intermediate

Too often, designs of FPGAs, ASICs, ASSPs, and other chips have negative impact on firmware development, causing schedule delays and lower quality in the embedded products being developed for market. Once a chip is in silicon form, it is generally too late to make RTL changes, causing the engineer to attempt workarounds in firmware to salvage the chip. This class teaches design practices in several areas of RTL design, such as documentation, registers, interrupts, aborts, and test hooks and makes it possible to more quickly develop the code, especially while debugging the interaction between the chip and firmware.

What You'll Learn: RTL design and style practices that will significantly help when writing firmware to control the chips.

Prerequisites: Understanding of chip design helpful.

Target Audience: RTL engineers designing chips. Firmware engineers writing firmware that controls these chips.

With: Gary Stringham

Tuesday, 8 March 2005

8:30am - 10:00am



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ETP-208 Debugging Elusive Digital Problems Quickly

Level: Intermediate

Debugging a digital system depends on being able to capture and analyze unique signal and event anomalies that are causing problems. These anomalies can be hard to find and capture. This class shows logic analyzer triggering techniques to find and capture these problems. Attendees learn how to trigger on errors such as clock glitches, crosstalk, termination errors, setup/hold violations, missing pulses, too narrow pulses, too long interrupt response times, power up configuration error, etc. These techniques will help capture bugs that threaten development schedule.

What You'll Learn: How to use the sophisticated trigger engine of modern logic analyzers to capture and analyze unusual circuit anomalies.

Target Audience: Embedded hardware developer and digital designers who are required to evaluate, troubleshoot and debug digital circuitry.

With: David Haworth

Tuesday, 8 March 2005
8:30am - 10:00am



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ETP-209 Short-Range Wireless Data Communications

Level: Introductory

A plethora of short-range wireless data communication solutions now vie for the attention of embedded designers. The current crop includes IrDA, Bluetooth, 802.11b, Ultra Wideband, HomeRF and more. These technologies cover a wide range of capabilities and constraints. Sometimes they compete and other times they complement. Who will win? Who will lose? Do there have to be winners and losers? This class provides a survey of the broad range of short-range wireless data communication technologies currently available for embedded devices.

What You'll Learn: An understanding of short-range wireless technologies that are currently available and the trade-offs inherent in each.

Target Audience: Designers of embedded systems with short-range wireless data communication components.

With: Charles Knutson

Tuesday, 8 March 2005
8:30am - 10:00am



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ETP-210 Noise and Shielding

Level: Intermediate

This class covers electromagnetic noise and how to design circuits and shielding to avoid it. It will present the sources of noise and the mechanisms for noise energy transmission and coupling. These mechanisms include conductive, inductive, capacitive, and electromagnetic couplings. The class includes methods for shielding and filtering noise. The topics include grounding, shielding, electrostatic discharge (ESD), general diagnostics, layout of signal traces, cables, and enclosures.

What You'll Learn: How to define, analyze, and select techniques for shielding circuits and subsystems from electrical noise.

Prerequisites: Basic understanding of electromagnetic propagation, magnetic coupling, electrostatic forces, current flow and impedance required.

Target Audience: Managers and engineers who want a technical basis for shielding their products.

With: Kim Fowler

Tuesday, 8 March 2005
8:30am - 10:00am



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ETP-220 Designing with Real-Time Kernels, Part 2

Level: Intermediate

This is the second class in a two-part series. Please see class ETP-200 for abstract.

With: Jean Labrosse

Tuesday, 8 March 2005

10:15am - 11:45am



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ETP-221 Effective Use Cases for Real-Time Systems

Level: Introductory

In the real-time and embedded domain, there are few references for how to effectively capture both the functional and quality of service requirements, so engineers in this domain are having a very difficult time effectively capturing requirements at the right level of detail. This class presents the approach the author has introduced at NASA/JPL for the capturing of the requirements for complex space mission requirements. This approach uses use cases, actors, sequence diagrams, and statecharts to capture requirements and then provides a means to track these requirements forward into the design of the system.

What You'll Learn: How use cases can structure requirements and how clear, unambiguous requirements can lead to robust testable designs.

Target Audience: Systems and software developers, requirements analysts

With: Bruce Powel Douglass

Tuesday, 8 March 2005
10:15am - 11:45am



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ETP-222 Principles of High Availability Embedded Systems Design, Part 2

Level: Introductory

This is the second class in a two-part series. Please see class ETP-202 for abstract.

With: David Kalinsky

Tuesday, 8 March 2005

10:15am - 11:45am



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ETP-223 TCP/IP for Embedded Engineers

Level: Intermediate

This class explains TCP/IP, using the OSI model. The physical, data link, network, and transport layers are introduced including the TCP and UDP transport protocols. Specific requirements for TCP/IP are discussed for common intended uses in embedded systems. Linux sources are widely available and it is free from license costs and includes a stable tested TCP/IP stack proven in server class machines. The class examines Linux and compares it to other implementations of TCP/IP often used in embedded systems. This class also covers IPv6 and security.

What You'll Learn: Preparation for making the choices faced in deploying TCP/IP in an embedded project.

Prerequisites: Basic understanding of programming techniques required.

Target Audience: Working engineers and managers who have an interest in TCP/IP or a need to deploy TCP/IP networking in their embedded design.

With: Thomas Herbert

Tuesday, 8 March 2005
10:15am - 11:45am



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ETP-224 Measuring Execution Time and Real-time Performance, Part 2

Level: Intermediate

This is the second class in a two-part series. Please see class ETP-204 for abstract.

With: Dave Stewart

Tuesday, 8 March 2005

10:15am - 11:45am



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ETP-225 Embedded Programming 101, Part 2

Level: Introductory

This is the second class in a two-part series. Please see class ETP-205 for abstract.

With: Michael Barr

Tuesday, 8 March 2005
10:15am - 11:45am



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ETP-226 Introduction to Posix Threads

Level: Introductory

The heavyweight "process model," historically used by Unix systems, including Linux, to split a large system into smaller, more tractable pieces, doesn't always lend itself to embedded environments owing to substantial computational overhead. POSIX threads, also known as Pthreads, is a multithreading API that looks more like what embedded programmers are used to but runs in a Unix/Linux environment. This class introduces Posix Threads and shows you how to use threads to create more efficient, more responsive programs.

What You'll Learn: An appreciation for the features of Posix threads as a tool for building robust and efficient programs.

Prerequisites: Fluency in C required.

Target Audience: This class is aimed at two audiences: 1. Unix/Linux programmers who need an introduction to the multi-threaded programming paradigm. 2. Programmers with a background in multitasking operating systems who want to apply lightweight multitasking in a Linux environment.

With: Doug Abbott

Tuesday, 8 March 2005
10:15am - 11:45am



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ETP-227 Basic Control Theory for the Software Engineer

Level: Advanced

The z transform is an essential part of a structured control system design. This class describes the basics of using the z transform to develop control systems, using the sort of math that is familiar to the accomplished embedded system designer.

What You'll Learn: Use the z transform to perform basic control systems analysis and design tasks.

Prerequisites: Some experience with closed-loop control systems recommended. Working knowledge of simple controllers, ability to read C code, and advanced algebra required.

Target Audience: Engineers and managers with experience implementing closed-loop control systems who want to approach the process in a more structured manner.

With: Tim Wescott

Tuesday, 8 March 2005
10:15am - 11:45am



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ETP-228 Introduction to the ANSI/EIA/CEA-709.1 Control Networking Protocol

Level: Introductory

The ANSI/EIA/CEA-709.1 control networking protocol is in use in more than 40 million devices that have been installed in homes, buildings, factories, trains, and other embedded systems worldwide. Key features of the protocol are described at each of the seven OSI reference model layers. The EIA-709.1 protocol is compared to TCP/IP. A free API for embedded system developers is presented that can be used to create EIA-709.1 applications for any embedded microcontroller. The API functions are described, as well as the effort required to port the API to a new processor and to add control networking to existing embedded applications.

What You'll Learn: Apply the ANSI/EIA/CEA-709.1 protocol to embedded applications that require network communication

Target Audience: Software and firmware developers who are developing embedded applications that are distributed among multiple processors and that require network communication. The class is also suitable for project managers, system engineers, and marketing professionals for these types of embedded applications.

With: Rich Blomseth

Tuesday, 8 March 2005
10:15am - 11:45am



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ETP-229 Wireless Protocol Stacks

Level: Advanced

This class concentrates on the details of wireless protocol stacks that are useful to engineers that need to dig deeper into the technology than the typical application programmer. The goal is to allow you to use these stacks to their fullest potential in the specialized systems you are designing.

What You'll Learn: The strengths and weaknesses of a variety of wireless protocols to make more informed decisions about designing wireless systems.

Prerequisites: Solid understanding of communications protocol stacks and General understanding of how wireless communications work.

Target Audience: Engineers who need a working knowledge of the internal workings of a variety of wireless protocol stacks.

With: Larry Mittag

Tuesday, 8 March 2005
10:15am - 11:45am



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ETP-230 Top Ten Usability Mistakes

Level: Introductory

In embedded user interfaces, the same mistakes appear again and again. A device with multiple modes confuses the user, or a screen times out just when the user is about to press a key. The text of the display uses terms that make sense to the engineer that designed the device but baffle the ordinary user. This class addresses these problems and looks at a set of examples of real products to identify the most common and easily eliminated usability mistakes.

What You'll Learn: How to identify and remove the most common mistakes made in the design of the user interface of an embedded device.

Target Audience: Engineers implementing user interfaces who have to design the interaction between user and device.

With: Niall Murphy

Tuesday, 8 March 2005

10:15am - 11:45am



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ETP-240 Inside Real-Time Kernels, Part 1

Level: Intermediate

This class examines the inner workings of a real-time kernel. Also known as an RTOS, it is software that manages the time of a microprocessor, microcontroller or DSP, allows multitasking, and provides valuable services to embedded applications. By understanding internals, you will have a better grasp on the issues involved when using a kernel. This class shows how a kernel works. You will experience the inner workings of a scheduler, see what's involved in a context switch, and examine how semaphores, message queues, and many other common kernel services are typically implemented. This is the first class in a two-part series.

What You'll Learn: What a kernel is and how it works.

Prerequisites: Knowledge of C and some knowledge of assembly language required.

Target Audience: Anyone who wants to quickly and deeply understand how an RTOS works in order to better select and use one.

With: [Jean Labrosse](#)

Tuesday, 8 March 2005
2:15pm - 3:45pm



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ETP-241 Design Patterns for Tasks in Real-Time Systems

Level: Intermediate

This class presents design patterns that are commonly used for partitioning an embedded systems application that run under a real-time operating system into tasks, with the goal of enabling programmers to apply them to their own work. These design patterns fall into three major groups: desynchronizing patterns, which partition the design into tasks that operate asynchronously to one another so that tasks can be prioritized; synchronizing patterns, which are used for controlling access to shared resources; and architectural patterns, which are used for implementing commonly occurring functional themes.

What You'll Learn: Guidelines for partitioning an embedded application into tasks under a real-time operating system.

Prerequisites: Familiarity with RTOS operation and knowledge of C required.

Target Audience: This class is targeted at embedded systems programmers that are familiar with the basics of Real Time Operating System (RTOS) operation who want to explore ways to partition an embedded application into tasks.

With: [Michael Grischy](#)

Tuesday, 8 March 2005

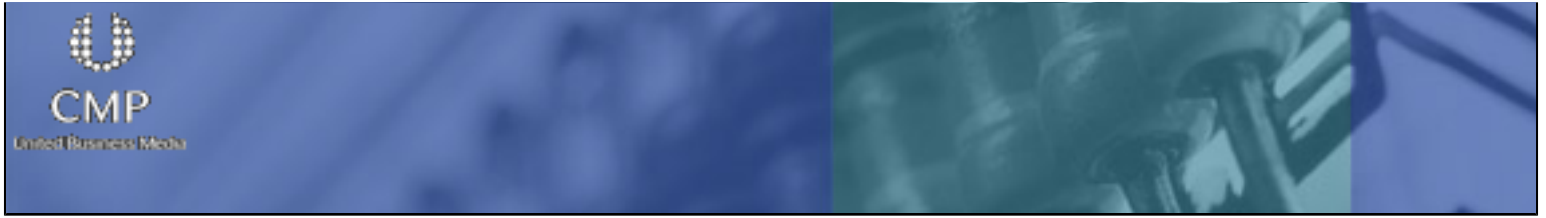
2:15pm - 3:45pm



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ETP-242 SysML: The New Systems Modeling Language

Level: Introductory

SysML is a new modeling language, heavily based on the UML 2.0 but significantly adding to and extending the UML. SysML provides continuous behavioral modeling and adds a number of new semantics concepts, such as parametric modeling, and several new diagram types. This standard is currently under development and will be released as a standard this year. This class reveals the internals of the SysML and how it can be used for effective systems development, as well as how systems designs can be efficiently passed on to software developers.

What You'll Learn: The basic semantic and notational elements in the upcoming SysML language for modeling systems requirements and designs.

Prerequisites: Some basic familiarity with the UML required.

Target Audience: Systems Engineers and Designers and software engineers working in a systems engineering environment

With: Bruce Powel Douglass

Tuesday, 8 March 2005
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ETP-243 Embedded Systems Programming Using DSPs

Level: Introductory

Developing embedded digital signal processing (DSP) applications is a complex task influenced by many parameters. But by using a systematic approach, the result can be an efficient implementation. This class provides an overview of application development techniques associated with DSPs in embedded systems. Topics include differences between DSPs and other general purpose processors, choosing a DSP for an embedded application, survey of DSP architectures, summary of tools for DSP application development, and real-time application development techniques using DSPs.

What You'll Learn: A familiarity with the concepts, techniques, and processes for developing DSP-based applications.

Target Audience: Embedded engineers, managers, and team leads that are new to the embedded DSP space and are looking for application development techniques specific to Digital Signal Processing.

With: Robert Oshana

Tuesday, 8 March 2005
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ETP-244 The 25 Most Common Mistakes with Real-Time Software Development, Part 1

Level: Introductory

This class presents the most common mistakes and pitfalls associated with developing embedded real-time software. The origin, causes, and hidden dangers of these mistakes are highlighted. Methods ranging from better education to using new technology and recent research results are also discussed. The mistakes vary from problems with the high-level project management methodologies to poor decisions on low-level technical issues relating to the design and implementation. This is the first class in a two-part series.

What You'll Learn: Recognize the most common problems encountered when building real-time systems and obtain an overview of methods and solutions to avoid making mistakes.

Target Audience: Anyone involved in building real-time embedded systems.

With: Dave Stewart

Tuesday, 8 March 2005

2:15pm - 3:45pm



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ETP-245 Embedded Linux Startup Code

Level: Advanced

This class is a walkthrough of the startup-related portions of the Linux kernel source code, from the point the kernel begins running until the kernel is ready to run user programs.

What You'll Learn: Linux's startup procedure, and how to modify that procedure when porting Linux to an embedded platform.

Prerequisites: Prior experience with the Linux operating system and programming in C required.

Target Audience: Embedded developers wanting information on porting Linux to an embedded platform.

With: William Gatliff

Tuesday, 8 March 2005

2:15pm - 3:45pm



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ETP-246 Memory Management, Part 1

Level: Intermediate

Use of memory in embedded systems must be measured to ensure the resources available are sufficient. The general purpose allocation mechanism available with most compilers can suffer from fragmentation, regardless of how carefully it is used. This is not acceptable for systems that have to run for long periods. Also a general purpose allocation scheme usually has undeterministic real-time properties as it may have to perform a search for memory of the appropriate size. This class looks at some custom alternatives that eliminate fragmentation and searches, such as fixed size pools. This is the first class in a two-part series.

What You'll Learn: How to evaluate the memory management options available to decide if malloc and free is appropriate for a project.

Prerequisites: Knowledge of C Programming required.

Target Audience: C programmers that use or are considering using a heap for dynamic memory management.

With: Niall Murphy

Tuesday, 8 March 2005
2:15pm - 3:45pm



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ETP-247 PID without a PhD

Level: Intermediate

The PID controller is a common control strategy used in many control loops in the world today. This class teaches how to design and implement a PID controller in software. It uses practical examples to show how the various elements of a PID controller affect system performance, it gives methods for implementing PID controllers including how to avoid some common pitfalls, and it gives the designer guidance in designing the controller up-front to help estimate the processor load and insure the hardware design is adequate to the task.

What You'll Learn: Design a closed-loop PID (Proportional, Integral, Derivative) controller.

Prerequisites: Ability to read C required.

Target Audience: Embedded systems designers and their managers who are or will be involved in designing closed-loop feedback control systems.

With: [Tim Wescott](#)

Tuesday, 8 March 2005
2:15pm - 3:45pm



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ETP-248 Managing Power, Ground, and Noise in Microcontroller and Analog Applications

Level: Intermediate

Microcontroller applications often have low-level sensor signals and moderate power drive circuitry, in addition to the microcontrollers. A peaceful co-existence with these three extremes requires careful power and ground distribution design. This class discusses sources of noise in all three areas and the paths where the noise travels around. It also discusses the proper selection and placement of noise isolating and limiting components to keep digital and power noise out of sensitive input circuits.

What You'll Learn: Good layout practices, their impact on noise, and the theory behind them.

Target Audience: This class is recommended for any designer who has struggled to keep digital and power noise out of sensitive input circuits, or is just curious about where all the black magic Rules of Thumb for board layout come from.

With: [Bonnie Baker](#)

Tuesday, 8 March 2005
2:15pm - 3:45pm



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ETP-249 Understanding and Using the 802.11 Standards

Level: Intermediate

This class examines the IEEE standards relating to wireless communications. The emphasis will be on what each standard means to working engineers creating embedded systems around wireless communications.

What You'll Learn: What standards are in process and what they mean to engineers creating wireless systems.

Prerequisites: Solid understanding of communications protocol stacks and a general understanding of how wireless LANs work.

Target Audience: Engineers who need a working understanding of the 802.11 standards and how they are developed.

With: Larry Mittag

Tuesday, 8 March 2005

2:15pm - 3:45pm



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ETP-250 Fantastic Failures

Level: Introductory

Failure can be the source of useful information. This class presents several case studies of failures and illustrates what went wrong, what we can learn, and what we can do to avoid them. The case studies include Comet - the first jet-engine airliner that tested the limits of human knowledge; Therac-25 - a development nightmare in system design; Chernobyl - a study in human expertise, experience, and arrogance; Apple Lisa - great ideas before their time, a marketing miscue; Product recalls; and Sidewinder missile - innovative development practices that led to a system that is still useful 50 years later.

What You'll Learn: Understanding the place of failure in designing new products.

Target Audience: Managers, team leaders, engineers, developers, or anyone involved in developing products.

With: Kim Fowler

Tuesday, 8 March 2005

2:15pm - 3:45pm



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ETP-260 Inside Real-Time Kernels, Part 2

Level: Intermediate

This is the second class in a two-part series. Please see class ETP-240 for abstract.

With: Jean Labrosse

Tuesday, 8 March 2005
4:00pm - 5:30pm



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ETP-261 Executable UML

Level: Introductory

Executable UML is here. When using the traditional approach of adding code to UML, a series of implementation decisions are made that may not be correct, appropriate, or even knowable. Executable UML changes all that by allowing for early verification through simulation of an UML. The model, once verified, can be translated directly into efficient code using an openly accessible, tunable model compiler.

What You'll Learn: The components of executable UML, how they fit together, translation into code, what decisions need to be made, and at what time during the process.

Prerequisites: Familiarity with UML required.

Target Audience: Senior developers, technical leads, embedded developers

With: Stephen J. Mellor

Tuesday, 8 March 2005
4:00pm - 5:30pm



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ETP-262 Leveraging Bit-Stream Encryption to Protect IP and Proprietary Designs

Level: Intermediate

Now that FPGAs offer performance and costs comparable to ASICs and ASSPs, with the additional advantages of low development risk, faster time to market and flexibility, they are increasingly being used for critical system functions. Protecting designs implemented in FPGAs is becoming more important. The latest generations of SRAM-based FPGAs use configuration bitstream encryption to secure designer's intellectual property (IP). This class discusses the various types of security threats to programmable logic devices and details encryption methodologies that can be used to protect proprietary designs and IP implemented in FPGAs.

What You'll Learn: How to implement an encryption scheme using programmable logic to protect against threats to proprietary IP and designs.

Prerequisites: Basic FPGA technology knowledge required.

Target Audience: Design Engineers

With: Jie Feng

Tuesday, 8 March 2005
4:00pm - 5:30pm



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ETP-263 Embedded Systems Development: A Cookbook Approach

Level: Intermediate

Building on previous presentations of SEEM, this class offers a detailed step-by-step approach for analyzing, designing and implementing an embedded system. A "cookbook" is presented that clearly delineates the sequence of SEEM artifact creation from problem description through implementation. The cookbook also describes tracking the dependencies among the artifacts, and the manner in which iteration is embraced in order to handle discovered bugs and changing requirements. SEEM's main hallmark--namely, traceability from an unambiguous problem definition to the implementation--is explicitly described.

What You'll Learn: Practical methods for architecting, designing, and developing embedded systems in a repeatable, reliable manner without introducing unwieldy process.

Prerequisites: Moderate development experience with an understanding of object-oriented architecture required.

Target Audience: The ideal participant will be a system architect, project manager or senior system developer.

With: Thomas A. Bullinger

Tuesday, 8 March 2005

4:00pm - 5:30pm



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ETP-264 The 25 Most Common Mistakes with Real-Time Software Development, Part 2

Level: Introductory

This is the second class in a two-part series. Please see class ETP-244 for abstract.

With: Dave Stewart

Tuesday, 8 March 2005
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ETP-265 Embedded Linux Interrupt Code

Level: Advanced

This class is a walkthrough of the interrupt-related portions of the Linux kernel source code, from the point an interrupt is asserted to the point the associated interrupt handler begins running. A brief look at how Linux interacts manipulates interrupt controller hardware is also provided.

What You'll Learn: An understanding of Linux's interrupt handling mechanism, and how to adapt that mechanism to an embedded platform.

Prerequisites: C programming and some experience with the Linux operating system required.

Target Audience: Embedded developers wanting information on porting Linux to an embedded platform.

With: William Gatliff

Tuesday, 8 March 2005
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ETP-266 Memory Management, Part 2

Level: Intermediate

When using malloc and free there is a danger that memory leaks will be introduced into your program. In the case where there is no memory leak, the programmer may still want to measure the amount allocated and freed to confirm that there is no problem. When there is a leak it is vital to identify the exact line where the allocation took place so that the bug can be fixed. Part 2 looks at debugging code that can be inserted into your program to give the programmer a measurement of heap use. This is the second class in a two-part series. Please see ETP-246 for the abstract for Part 1.

With: Niall Murphy

Tuesday, 8 March 2005

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ETP-267 Building Signaling Platforms with ATCA

Level: Intermediate

The Advanced Telecom Computing Architecture (ATCA) defines a managed platform for building modular, flexible, scalable platforms for Telecom applications. The ATCA specification includes the Advanced Mezzanine Card (AMC), hot-swappable modules that provide I/O (from T1/E1 up to Optical OC3/OC12 interfaces) or processing capability. Signaling and other networking protocols may be implemented on the I/O modules. Upper layers or call processing applications may be implemented on processing modules. Even voice processing is possible. This class describes how to construct scalable signaling platforms with ATCA.

What You'll Learn: How to construct scalable signaling platforms, using the modularity of ATCA and well-structured protocol stacks.

Target Audience: Attendees of this class should be systems engineers, architects and managers in the telecom field, who are responsible for designing signalling platforms using SS7 and Next Generation signalling protocols, such as Sigtran

With: James Darroch

Tuesday, 8 March 2005
4:00pm - 5:30pm



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ETP-268 An Introduction to eCos

Level: Intermediate

eCos is an open source, royalty free operating system for embedded and real-time applications. It is highly configurable to allow only those features of the OS that are required for an application to be built into the executable. eCos attempts to fill the gap between buying a commercial RTOS and building it yourself. The class includes an introduction to the features supported by eCos and a demonstration of the configuration and building of an eCos system.

What You'll Learn: A basic understanding of eCos, how to configure it for different platforms and how to write and build programs that use it.

Prerequisites: Understanding the role of system software in embedded systems and familiarity with embedded hardware assumed.

Target Audience: This session will be of benefit mainly to Engineers and Technical Managers.

With: Nick Garnett

Tuesday, 8 March 2005

4:00pm - 5:30pm



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ETP-269 802.11 Security

Level: Advanced

This class examines the options for securing wireless communications. Special attention will be paid to the evolving standards for wireless LANs, including AES and 802.11i.

What You'll Learn: The strengths and weaknesses of a variety of security options for wireless communications and just how secure wireless communications can be.

Prerequisites: Understanding of communications protocol stacks and how wireless LANs work required.

Target Audience: Working engineers that need to build robust security into their wireless communications will derive the most benefit from this session.

With: Larry Mittag

Tuesday, 8 March 2005
4:00pm - 5:30pm



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ETP-270 Mission-Critical and Safety-Critical Development

Level: Introductory

This class covers issues in designing mission-critical and safety-critical systems. It provides the general processes used in design and development and illustrates them with two case studies: a satellite subsystem and a medical device. The topics cover the various aspects: the phases of development, documentation, plans, procedures, reviews, and reports. The class also addresses concerns over version control, archiving, traceability, and audits.

What You'll Learn: The standards, processes, and documentation needed for developing safety-critical and mission-critical systems.

Target Audience: Managers, engineers, and developers wanting to learn about the development of medical devices, satellites, military equipment, or avionics.

With: Kim Fowler

Tuesday, 8 March 2005
4:00pm - 5:30pm



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ETP-300 Secure Embedded OS: A Technology Overview

Level: Intermediate

One of the critical components involved in ensuring the security of embedded devices is the embedded OS. The security of an embedded device is extremely dependent on the ability of the OS to provide a secure environment for applications. This class provides an overview of the technology issues involved in designing a "Secure Embedded OS," and the implications of using it in secure embedded applications. Conformance to open standards is reviewed as well as process methodologies needed for secure OS development.

What You'll Learn: Understand security problems in embedded operating systems and how to evaluate the security capabilities of an OS.

Prerequisites: Basic understanding of RTOS internals and familiarity with processor architecture and software life-cycle & process methodology required.

Target Audience: The target audience includes engineers and managers who need to understand technology issues involved in designing security for embedded applications.

With: Arun Subbarao

Wednesday, 9 March 2005

8:30am - 10:00am



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ETP-301 Writing Your First WinCE USB Device Driver

Level: Introductory

The information required to write a USB device driver is plentiful, if you have the time and patience to find it. This class demonstrates, through the use of a practical example, a simple approach to writing a WinCE 5.0 USB device driver. The example includes the basic structure and requirements for implementing a device driver for a commercially available USB fingerprint sensor. The approach details how to write a WinCE stream driver, how to communicate via USB bus, how to install the driver on a platform, and how to ensure proper communication between the application and the device driver.

What You'll Learn: The basic information required to implement a WinCE 5.0 USB device driver.

Prerequisites: Basic understanding of C required.

Target Audience: This class provides new and intermediate developers with the background that they need to implement USB device drivers for the WinCE O/S.

With: Joe Tykowski

Wednesday, 9 March 2005
8:30am - 10:00am



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ETP-302 DODAF and the UML

Level: Intermediate

The Department of Defense Architecture Framework (DODAF) is a new standard, based upon the older C4ISR standard and specifies a semantic framework for representing architectures in a consistent way. The UML is a general modeling language but is particularly adept at clearly showing architectures, system structures, and behavior--all vital aspects of any DODAF-compliant product. The class demonstrates how useful and appropriate the UML is at creating both the required and supporting DODAF products.

What You'll Learn: The basic concepts of the DODAF standard and the set of products specified in the standard, and how each may be represented with the UML.

Prerequisites: Some basic familiarity with the UML required.

Target Audience: Systems and software developers, project leads and managers wanting to design systems against the new DODAF standard

With: Bruce Powel Douglass

Wednesday, 9 March 2005
8:30am - 10:00am



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ETP-304 Implementing High Availability with the SA Forum Specifications

Level: Intermediate

The Service Availability Forum has published specifications for common APIs and methods for ensuring services remain available in an environment where uptime must be maintained at least at levels of 99.999% capacity. The SA Forum specifications cover the interfaces between the hardware layer and upper layers and the interfaces providing high availability services to the applications, application services and other middleware, referred to as the Application Interface Specification (AIS). An open source software implementation of AIS services is examined to understand how the specifications are applied in real applications.

What You'll Learn: How systems using the Service Availability Forum specification are implemented.

Target Audience: Aimed at designers and developers of embedded systems requiring High Availability for applications deployed in environments such as communication network equipment where uptime requirements dictate special attention to keep service available at all times.

With: Steven Dake

Wednesday, 9 March 2005
8:30am - 10:00am



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ETP-305 C and C++ Gotchas, Part 1

Level: Intermediate

Static checking in C catches many potential errors at translation time that might otherwise become run-time errors. C++ applies even stricter checks to weed out more errors at translation time. Nonetheless, C and C++ programs can still have "gotchas"--constructs that compile and link without diagnostics, yet produce unintended, and often disastrous, run-time results. This class explains why gotchas are an inherent part of C and C++. It presents numerous platform-independent C and C++ programming examples containing gotchas and, when possible, recommends ways to avoid them. This is the first class in a two part-series.

What You'll Learn: How to anticipate and avoid gotchas in C and C++ programs.

Prerequisites: C and C++ programming experience required.

Target Audience: C and C++ programmers

With: Dan Saks

Wednesday, 9 March 2005
8:30am - 10:00am



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ETP-306 Optimizing C for Embedded Systems

Level: Intermediate

This class presents several techniques used for optimizing software in embedded systems. The focus is on embedded systems programmed using the C language, however, the techniques presented are applicable to any software development in any software language. The topics presented are: optimization trade-offs, rules of optimization, generic optimization techniques for embedded systems, and compiler optimizations.

What You'll Learn: Optimization of embedded software applications for maximum performance and minimum memory requirements.

Prerequisites: A good understanding of hardware/software interactions required.

Target Audience: The intended audience for this class is experienced embedded systems software engineers who desire a deeper understanding of program optimization and its impact on system performance.

With: Ted Schleich

Wednesday, 9 March 2005

8:30am - 10:00am



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ETP-307 Internet Messaging and Mail Protocols

Level: Intermediate

While SMTP, The Simple Mail Transfer Protocol, is the most widely used messaging protocol, there are others that can be used. This class presents the fundamentals of SMTP as well the the POP (Post Office Protocol) and IMAP (Interactive Mail Access Protocol) used in user mail handling. Two message protocols, SYSLOG and SNMP Traps are also presented which provide devices with the ability to send machine to machine messages. Understanding the variety of methods available for asynchronous message delivery will enable designers to chose the methods appropriate for their systems.

What You'll Learn: The fundamentals of the primary mail protocols SMTP, POP and IMAP and how these protocols can be leveraged in embedded devices.

Target Audience: System and firmware engineers working on network appliances and other networked devices who wish to understand the various messaging and mail protocols that can be used in TCP/IP systems for events e-mail and other messaging applications.

With: Christopher Leidigh

Wednesday, 9 March 2005
8:30am - 10:00am



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ETP-308 IP Version 6 and the Dual Stack

Level: Intermediate

Internet Protocol version 6 (IPv6) improves on IPv4 by greatly increasing the number of available addresses and by enabling more efficient routing, simpler configuration, built-in IP security, better support for real-time data delivery, and other essential enhancements. Almost all of the transition mechanisms from IPv4 to IPv6 require the need for a host to run a dual stack: IPv4 and IPv6 together. Attendees are exposed to the challenges an embedded system engineer designing an IP enabled device faces when implementing an IPv6 or dual stack in terms of resources and performance.

What You'll Learn: An understanding of IP version 6 features, benefits and new protocols, their interactions and inter-relations.

Prerequisites: Binary and hexadecimal notation system, IP version 4 addressing scheme and Ethernet LAN required.

Target Audience: Embedded system designers needing to understand IP version 6 networking in order to embed it in their products.

With: Christian Legare

Wednesday, 9 March 2005

8:30am - 10:00am



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ETP-309 Designing with Soft Processor Cores in FPGAs, Part 1

Level: Introductory

This class presents an overview of Soft Processor Core (SpC) technology, vendors, choices, performance, toolsets and design flows for programmable logic. An overview of the architectural elements of RISC processors provides the required foundation for the comparison of current vendor SpC offerings. SpC design flows are presented along with common design challenges and potential solutions. The advantages, disadvantages, flexibility and performance of soft vs. hard processors is discussed. Analysis and system requirement prioritization is reviewed to help designers perform efficient trade-off evaluations of potential SpC implementations. This is the first class in a two-part series.

What You'll Learn: Soft processor core architectures, benefits, costs, design flow, design challenges and mitigations, current vendor offerings and system requirement allocation for efficient design evaluation.

Target Audience: Engineers or managers evaluating or implementing projects which may include a soft processor core implemented within an FPGA

With: RC Cofer / Ben Harding

Wednesday, 9 March 2005
8:30am - 10:00am



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ETP-310 How to Streamline Embedded Systems Development with Eclipse

Level: Introductory

Model Driven Architecture offers big gains for embedded systems developers, but the problem of integrating the tools required for MDA has not yielded a simple solution. Developers need a UML editor, a transformation engine, a compiler, and a code debugger. A model-level debugger and hardware simulators also aid the process. Eclipse, an open source framework, can solve some of these integration problems and streamline the development process. This class explains how Eclipse helps embedded systems developers with design, model transformation, debugging, and system deployment.

What You'll Learn: Learn how to integrate the tools required for MDA and deploy a simple embedded system from the Eclipse framework.

Target Audience: This session is tailored to two groups of practitioners: (1) those who want to explore the possibilities that Eclipse creates for embedded systems developers, and (2) teams that would like to use Model Driven Architecture in their own projects. Embedded systems engineers and project managers can benefit from this session if they are:

- Interested in learning how to use the Eclipse framework in embedded systems development.
- Acquainted with Model Driven Architecture (MDA) and would like to apply it to development of their own systems.
- Eager to learn innovative ways to improve embedded systems development.

With: Jason Wilson, Steven Greffenius

Wednesday, 9 March 2005
8:30am - 10:00am



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ETP-320 Designing Applications for Symmetric Multi-Processing Systems

Level: Intermediate

This class presents the design issues you face when porting an existing application to an SMP system or designing a new application to take advantage of SMP hardware. It covers hardware constraints, including bandwidth limits and I/O subsystem performance, with examples of how these constraints can be removed or minimized with specialized hardware elements. A discussion follows on how the operating system and applications can be architected to maximize performance on an SMP system. Specific examples of application re-architecting using optimization tools will be shown.

What You'll Learn: An understanding of SMP hardware architectures, operating system support for SMP, and design of applications.

Target Audience: The target audience for the class are embedded system developers with an interest in adopting SMP architectures as the basis for future designs.

With: Robert Craig and Bob Behrooz, Field Application Engineer, Freescale Semiconductor

Wednesday, 9 March 2005

11:00am - 12:30pm



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ETP-321 AVR Microcontroller for Control Application Developments

Level: Intermediate

Typical AVR microcontroller applications are sensing, motion control, lab automation, and equipment/instrument controls. Mechanical systems typically have less than 10-khz bandwidth. AVR microcontrollers, clocking at 4 to 16 MHz, can facilitate fairly extended and robust real-time control for these systems. This class presents an overview of an AVR-based application prototyping and development environment and process. It then describes the AVR architecture, instruction set, C and assembly coding introduction. The class covers simulation and hardware emulation, with examples.

What You'll Learn: Ability to formulate quick HW/SW prototyping solutions for sensing, motion control, lab automation, and equipment/instrument control.

Prerequisites: Basic understanding of digital hardware interface, ADC/DAC, real-time timer/counter, and RISC architecture/instruction set required.

Target Audience: This class is intended for application developers who are working on sensing, motion control, lab automation, and equipment/instrument control projects.

With: Joe-Ming Cheng

Wednesday, 9 March 2005

11:00am - 12:30pm



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ETP-322 Understanding Compilers and Optimizations for Embedded Systems

Level: Introductory

Embedded systems are increasingly being programmed in higher level languages like C/C++ and Java. The benefits include portability, maintainability and productivity, but there can also be drawbacks. It is useful to understand how a high level language program is translated into instructions and when you cannot rely on the compiler! This class overviews the compilation process, discusses some basic compiler optimization techniques that can help you meet your performance goals, and reviews some of the more advanced techniques that allow you to perform more global or program level optimizations.

What You'll Learn: Various techniques used to improve embedded application performance using a combination of tools, algorithms, and architectures.

Prerequisites: Basic understanding of software build tools required.

Target Audience: This class is intended for engineers, managers, and team leads who are looking for techniques and tactics for extracting full technology entitlement from their embedded application.

With: Robert Oshana

Wednesday, 9 March 2005

11:00am - 12:30pm



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ETP-323 Wireless Embedded Networks: Connectivity for Everyday Objects

Level: Introductory

The ever-decreasing cost and increasing performance of silicon Radio Frequency Integrated Circuits (RFICs) makes it practical to manufacture wireless communication capabilities into everyday goods. With the addition of appropriate control software, simple RFICs can become store-and-forward nodes in device networks, giving rise to a new category of wireless embedded networking, to add sensing and control to everyday devices. This class covers the technology that makes wireless embedded networks possible, and how it will help drive the RFIC market in the future.

What You'll Learn: Embedded network architectures and how they differ from conventional wireless LAN systems, including the benefits gained by a self-organizing, self-healing mesh architecture.

With: Robert Poor

Wednesday, 9 March 2005
11:00am - 12:30pm



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ETP-324 Web Services in Embedded Systems

Level: Introductory

Web Services are key to the harnessing of the power of Internet connected embedded devices. They are the preferred method of calling remote procedures and enabling distributed computing for both embedded and business systems. This class provides an introduction to Web Services--what they are, the standards behind them (XML, SOAP, WSDL and UDDI) and their advantages and disadvantages for the embedded world. Some real world examples of Web Services are discussed.

What You'll Learn: An understanding of what Web Services are, and how they can be implemented in systems ranging from 8-bit to 32-bit.

Target Audience: Design Engineers and Managers who are responsible for creating Networked Embedded systems

With: John Canosa

Wednesday, 9 March 2005
11:00am - 12:30pm



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ETP-325 C and C++ Gotchas, Part 2

Level: Intermediate

This is the second class in a two-part series. Please see class ETP-305 for abstract.

With: Dan Saks

Wednesday, 9 March 2005
11:00am - 12:30pm



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ETP-326 Modeling and Simulation Using UML, Part 1

Level: Intermediate

As programming languages turn into modeling languages, projects are being able to model systems at a high enough level of abstraction that allows for architecture validation using simulation. The ability to perform architecture validation and simulation is key to the success of current large programs that tend to span across multiple sites and companies. Standards such as the OMG's UML 2.0 and SysML are enabling technologies that allow organizations to effectively deploy simulation strategies that bridge across system and software teams. This is the same technology allows for team in differnt companies or locations to use a standard notation and delay implementation decisions until later in the program. An understanding of how to generate production level software from the same models that the systems engineers use for architecture, validation, and simulation. This is the first class in a two-part series.

What You'll Learn: A preview of the anticipated OMG standard on System UML and how the standard relates to executable UML.

Prerequisites: Knowledge of UML and simulation concepts required

With: Raetta Towers

Wednesday, 9 March 2005
11:00am - 12:30pm



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ETP-327 The Ten Secrets of Debugging Embedded Systems

Level: Intermediate

Developers of embedded software face unique challenges, including devices that must run for months without crashing, extreme reliability, and limited memory and processing power. To build cost-effective systems, embedded programmers must squeeze performance and find errors before they reach the field. From seeking the needles in the haystack to understanding where CPU cycles are truly wasted, this class will summarize years of experience with thousands of real-world systems into ten simple rules for building better real-time software.

What You'll Learn: How to identify and test for ten common issues in embedded and real-time systems such as memory leaks, performance bottlenecks, and API misuse.

Prerequisites: Knowledge of C or C++ required.

Target Audience: Embedded software engineers who want to know more about the inner workings of the tools they use.

With: Lori Fraleigh

Wednesday, 9 March 2005

11:00am - 12:30pm



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ETP-328 Networking Technologies for Low-Level Embedded Systems

Level: Intermediate

There are a very large number of networking technologies suitable for networking embedded systems. The focus of this class is to narrow down the choices by examining five networking technologies (serial, Bluetooth, LonWorks, Ethernet, and wireless Ethernet) relative to low-level embedded systems. The class presents overviews, definitions, evaluation metrics, networking technologies, and conclusions.

What You'll Learn: How to evaluate networking technologies for inclusion into low-level embedded systems.

Prerequisites: Good understanding of embedded systems design required. Computer networking knowledge is not necessary.

Target Audience: The intended audience of this class is anyone planning to network low-level embedded systems.

With: Ted Schleich

Wednesday, 9 March 2005
11:00am - 12:30pm



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ETP-329 Designing with Soft Processor Cores in FPGAs, Part 2

Level: Introductory

This is the second class in a two-part series. Please see class ETP-309 for abstract.

With: RC Cofer / Ben Harding

Wednesday, 9 March 2005

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ETP-330 Really Real-Time Systems

Level: Intermediate

Most smaller embedded systems meet their real-time requirements only by luck. We have few techniques that help us design a system that will be timely and predictable. This class shares practical (no UML, no academic proofs) ways to include time in your design, to help you produce a system that meets its deadlines, rather than beating a slow system into submission late in the debug stage. We examine the real speeds of common C constructs on various 8- and 16-bit CPUs, as well as faster alternatives to some compiler-supplied library routines.

What You'll Learn: Structuring code to meet performance requirements.

Prerequisites: Any assembly language and C required.

Target Audience: Anyone building resource-limited real-time systems.

With: Jack Ganssle

Wednesday, 9 March 2005

11:00am - 12:30pm



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ETP-340 Introduction to Distributed Embedded Systems

Level: Introductory

This class introduces the basic technical (and a few business) concepts behind developing a distributed embedded system in contrast to the typical centralized or single processor approach. The primary focus is at the architectural or product application level with an emphasis on the distributed function, partitioning, transfer dialogs, and the choice of communication protocol. Many real world examples in the automotive electronics industry are shown. The class also examines the business aspects of "going distributed," the basic process of developing a distributed product, and the importance of systems engineering.

What You'll Learn: Technical fundamentals and related business aspects that surround the development of a distributed embedded system.

Prerequisites: Basic background in computer science, computer engineering, or product design using microcontrollers assumed.

Target Audience: Product system, software, and hardware designers who are interested in transitioning from a centralized to a distributed product architecture.

With: [Bruce Emaus](#)

Wednesday, 9 March 2005

2:00pm - 3:30pm



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ETP-341 Case Example: Implementing DSPs in Biometric Systems

Level: Introductory

This class discusses the design decisions behind the development of a self-contained fingerprint-authentication device based on a digital signal processor. The discussion evaluates the selection of an appropriate processor and sensor, as well as the necessary verification software.

What You'll Learn: Maximize the capabilities of a DSP for image enhancement and minimize power consumption without sacrificing performance.

Prerequisites: Basic understanding of DSPs, semiconductors and Biometrics market a plus.

Target Audience: Design engineers interested in processor technologies for systems that require significant image enhancement capabilities and power management, such as fingerprint authentication devices

With: Ram Sathappan

Wednesday, 9 March 2005
2:00pm - 3:30pm



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ETP-342 Production Code Generation

Level: Introductory

With production code generation, code is automatically generated from executable models and deployed in embedded system products. Automotive and aerospace companies are quickly incorporating production code generation into their mainstream development processes for embedded control systems. Other industries and applications are assessing if production code generation is suitable for them. This class introduces model-based design and production code generation with emphasis on best practices and lessons learned from industry adopters. Topics detailed include code efficiency optimizations, data management, style guidelines, software integration, and verification and validation.

What You'll Learn: How to design, implement, and deploy embedded systems using a modeling environment and automatic code generation.

Prerequisites: Basic understanding of C required. Prior model-based design usage a plus (e.g., Simulink).

Target Audience: Systems and Software engineers developing complex embedded control systems utilizing or considering Model Based Design technology.

With: Tom Erkinen

Wednesday, 9 March 2005

2:00pm - 3:30pm



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ETP-343 FPGA Design for Firmware Engineers, Part 1

Level: Introductory

Many of today's fast turn embedded projects can benefit from the flexibility of FPGA technology. FPGA design flows are evolving and are increasingly similar to traditional software development flows. Hardware Description Languages (HDLs) are being used in place of schematic capture to define, simulate and verify design functionality. This class details an HDL-based FPGA design flow to engineers without an extensive hardware background. It presents an overview of FPGA technology and covers design decisions, including evaluation and selection of FPGA supplier, family, package and component. This is the first class in a two-part series.

What You'll Learn: The required foundation for designing with FPGAs, from evaluating and selecting an FPGA manufacturer to understanding the software tools.

Target Audience: Engineers or managers without extensive hardware experience evaluating or implementing a project utilizing FPGA technology.

With: RC Cofer / Ben Harding

Wednesday, 9 March 2005
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ETP-344 Real-Time Application Profiling for Improved Processor Utilization

Level: Intermediate

Accurate measurement of processor utilization can be critical for successful development of a complex real-time network application. A third party profiler may not be available in some cases, for instance, when no RTOS is running on a target system. This class gives an overview of the two most common profiling techniques, code instrumentation and sampling, and then shows how the code instrumentation can be used to measure processor utilization. The focus is on a case of a packet processing application running on a network processor.

What You'll Learn: How to accurately measure processor utilization for each task of your application without the use of a third party profiler and how to optimize your code to make it run faster.

Prerequisites: Knowledge of C and familiarity with constraints of embedded and real-time applications required.

Target Audience: Embedded real-time application developers. The class is especially useful to people who develop network applications with mandatory "line rate" throughput.

With: Vitaliy Slobotskoy

Wednesday, 9 March 2005

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ETP-345 Representing and Manipulating Hardware in Standard C and C++

Level: Intermediate

In addition to being used to develop highly portable applications, C and C++ can be used to write hardware-specific code. This class examines the features of standard C and C++ that can be used to represent hardware as data structures. It describes the common idioms for controlling typical devices, focusing on what can be done using only standard language features. It suggests platform-specific extensions that may be needed to complete the job. It also explores techniques for packaging hardware as abstractions.

What You'll Learn: Writing data declarations that accurately model hardware registers, and using the const and volatile qualifiers to improve the correctness and efficiency of device drivers.

Prerequisites: C and some C++ programming experience required.

Target Audience: Programmers seeking better ways to write device driver code.

With: Dan Saks

Wednesday, 9 March 2005
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ETP-346 Modeling and Simulation Using UML, Part 2

Level: Intermediate

This is the second class in a two-part series. Please see class ETP-326 for abstract.

With: Raetta Towers

Wednesday, 9 March 2005
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ETP-347 Slow Process Control: A Modeling/ Simulation Approach

Level: Advanced

Running a numeric simulation on a process model may accelerate the tuning of slow control systems: computer simulations with different controller architectures and/or with different parameters can be easily and quickly performed. Another advantage is the ability to predict the behavior of the controlled process before having a controller prototype to tune and test. This class provides some generalities on system modeling and model identification, and then focuses on a model structure especially suitable for the digital control of single-input/single-output linear systems. An identification algorithm is detailed.

What You'll Learn: Speed up the design and tune process and prediction of the behavior of the controlled process before having a controller prototype.

Prerequisites: System control theory and matrix algebra required.

Target Audience: Control system engineers who want to improve their design skills.

With: Ugo Ruggeri

Wednesday, 9 March 2005
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ETP-348 Embedding SSL: Internet Security for 8-bit Systems

Level: Intermediate

This class discusses the basics of SSL and Transport Layer Security (TLS, the IETF standard for SSL) and the problems inherent in constructing an SSL implementation for a system with limited resources, including processing requirements for encryption, digital certificate management, memory management issues, and seamless API integration with existing networking protocols. Real-world issues are illustrated by covering a working implementation of an SSL server for the Rabbit microprocessor.

What You'll Learn: Cryptography as it applies to SSL, the basics of the SSL protocol and the issues involved in implementing SSL for embedded systems.

Prerequisites: Understanding of network programming and TCP/IP, and the role of network security in embedded systems required.

Target Audience: This class is targeted at software and hardware engineers and managers interested in Internet security for embedded systems using the Secure Sockets Layer. A basic knowledge of network (TCP/IP) programming is assumed, but cryptography and security experience is not necessary.

With: Timothy Stapko

Wednesday, 9 March 2005

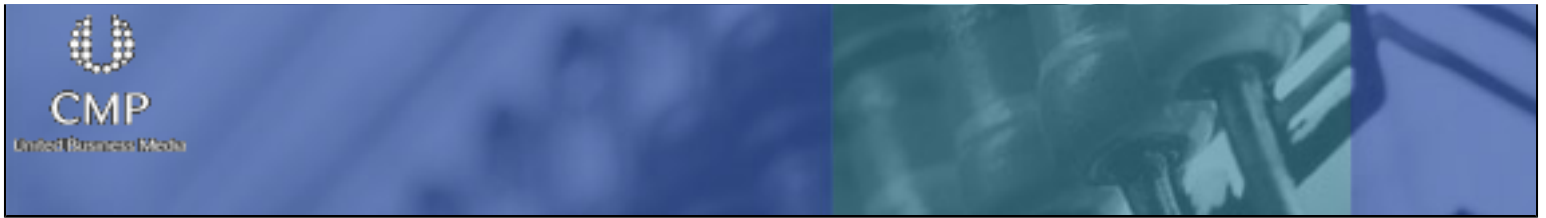
2:00pm - 3:30pm



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ETP-349 Pervasive Computing Applications and Wireless Sensor Networks

Level: Introductory

A new generation of applications that consist of dozens to thousands of tiny processing units is emerging, called pervasive computing. Potential applications include machine health and diagnostics, physiological monitoring, environmental monitoring, asset and inventory management, smart agriculture, and many more. The key enabling technology for these applications is the advent wireless sensor networks that merge ultra-low-power communication with miniaturization of sensors and actuators. In this class both the benefits and the many new challenges for embedded system engineers are discussed.

What You'll Learn: The many trade-offs that need to be considered when putting together a wireless sensor network or a pervasive computing application.

Target Audience: Application engineers and software engineers who anticipate or are planning to build distributed embedded applications using wireless sensor network technology.

With: [Dave Stewart](#)

Wednesday, 9 March 2005
2:00pm - 3:30pm



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ETP-350 Learning from Disaster

Level: Intermediate

Civil engineers have learned how to avoid failure from their rich history of bridge collapses, tunnel floodings, and building disintegrations. The firmware world is quite different; it seems we all make the same mistakes, repeatedly. Yet most problems have similar root causes. In this class a number of embedded disasters are examined, large and small, and lessons we must learn to improve our code are extracted.

What You'll Learn: Attendees will learn the most common mistakes that lead to product failures in the field.

Target Audience: Any developer afraid of having 60 Minutes appear at their office after deploying a new product.

With: Jack Ganssle

Wednesday, 9 March 2005
2:00pm - 3:30pm



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ETP-360 Verification and Validation for Embedded Software

Level: Introductory

Building quality into software during development is far more effective than trying to test it in after it's been built. Verification and validation techniques can be applied throughout the process lifecycle to help assure that the right product is being built, and the product is being built right. This class introduces the fundamental theory and techniques of verification and validation and discusses how these techniques have been successfully applied in the creation of high-quality embedded software.

What You'll Learn: The fundamental principles of verification and validation and the positive role they can play in the creation of high quality software systems.

Prerequisites: Understanding of software development and quality issues required.

Target Audience: Software developers for embedded systems.

With: Charles Knutson

Wednesday, 9 March 2005
3:45pm - 5:15pm



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ETP-362 Programming Frameworks for Embedded Multimedia Applications

Level: Intermediate

With the availability of high-performance embedded media processors, software engineers must port media-based algorithms from the PC environment to a realm where memory size and data bandwidth are important considerations. This class discusses programming frameworks that allow software developers to achieve the highest performance for a given application without increasing the complexity of the programming model. It also presents strategies for partitioning processor resources in single-core and dual-core media processors.

What You'll Learn: Different multimedia system frameworks and strategies for partitioning processor resources in single-core and dual-core media processors.

Prerequisites: Basic understanding of embedded processor architectures required, emphasizing memory and DMA subsystems.

Target Audience: Software developers who need to understand how to partition multimedia algorithms on embedded processors, where memory and bandwidth resources are more limited than in traditional PC-based applications.

With: [David Katz](#), [Rick Gentile](#), [Tomasz Lukasiak](#)

Wednesday, 9 March 2005

3:45pm - 5:15pm



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ETP-363 FPGA Design for Firmware Engineers, Part 2

Level: Introductory

This is the second class in a two-part series. Please see class ETP-343 for abstract.

With: Ben Harding, RC Cofer

Wednesday, 9 March 2005
3:45pm - 5:15pm



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ETP-364 Guidelines for Writing Portable Code

Level: Intermediate

Today's fastest, lowest power processor may be outdated tomorrow, leaving the developer locked into obsolete technology, unable to move to a new processor. Writing portable code can help minimize the risk by making the migration to newer processor or software technology as painless as possible. This class focuses on coding guidelines that take nothing for granted, leaving the programmer with a portable code base, ensuring access to the latest technology.

What You'll Learn: How to write portable C or C++ code.

Prerequisites: Basic knowledge of C required.

Target Audience: Embedded developers or managers of teams who program in C or C++.

With: Greg Davis

Wednesday, 9 March 2005
3:45pm - 5:15pm



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ETP-365 Writing ISRs in C++

Level: Intermediate

Writing hardware interrupt service routines (ISRs) entirely in Standard C++ is practically impossible. ISR calling conventions rarely, if ever, match normal C++ function calling conventions. When writing ISRs in C++, you must either dip into assembly language or use platform-specific language extensions. (Standard C is equally inadequate for writing ISRs.) This class shows you how to write much (just not all) of your ISR code in Standard C++. Attendees learn to use language linkage (e.g., extern "C") when interfacing C++ with hardware resources and assembly language code.

What You'll Learn: Implement an ISR framework in C++ and evaluate tradeoffs between performance and flexibility, particularly regarding choices between static and dynamic binding.

Prerequisites: Basic knowledge of writing device drivers in C++ required.

Target Audience: C++ programmers seeking better ways to write device driver code.

With: Dan Saks

Wednesday, 9 March 2005

3:45pm - 5:15pm



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CMP

United Business Media

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ETP-366 Building and Implementing Concurrent Specifications

Level: Introductory

Many requirements documents are described in a linear manner, which makes for "interesting times" when the system is highly concurrent and multi-threaded. Any attempt to take concurrency and distribution into account when expressing requirements can easily lead to premature design and difficulties in retargeting the application to a different environment. This class describes an approach to capturing concurrency in requirements as models and providing rules to sequentialize and sequence them in an implementation on an RTOS.

What You'll Learn: How to express requirements so they can be mapped easily to a multi-tasking/multi-threaded RTOS.

Target Audience: System engineers, software managers, project leads, embedded developers

With: Stephen J. Mellor

Wednesday, 9 March 2005

3:45pm - 5:15pm



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ETP-367 FPGA Embedded Processors: Revealing True System Performance

Level: Intermediate

This class investigates the performance and cost trade-offs for several FPGA embedded processor systems and gives an overview of the available peripherals and memory controllers. Several case studies examine the effects of various embedded processor memory structures and peripheral sets. The results from these case studies are used to draw conclusions regarding the performance and cost penalty incurred by using specific peripherals and memory architectures. After this class, attendees will understand how to interpret the manufacturers published benchmarks and how that translates into an actual system design.

What You'll Learn: Advantages and disadvantages of designing with an FPGA embedded processor; specifically, the tradeoffs between cost, memory architecture, peripheral set, and performance.

Prerequisites: Familiarity with FPGAs required. FPGA embedded processor design experience recommended.

Target Audience: The presentation is targeted at the embedded hardware and software engineer interested in designing with an FPGA embedded processor. Familiarity with embedded processor design is recommended.

With: [Bryan Fletcher](#)

Wednesday, 9 March 2005

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ETP-368 Power Optimization Techniques for Embedded Systems Programmers

Level: Introductory

Relatively little emphasis has been placed on power optimization techniques that can be applied to embedded system applications. This class provides an overview of basic static and dynamic power optimization techniques that can be used to reduce power consumption in portable embedded applications. The power optimization process is discussed to show how to select the right device, how to build an application to optimize power consumption, and how to measure and optimize for power after the application is built.

What You'll Learn: Practical power optimization techniques the process to follow when developing power efficient applications.

Prerequisites: Basic understanding of processor architectures and a high level programming language such as C/C++ required.

Target Audience: The target audience for this class are embedded programmers, team leads, and managers who are looking for practical techniques for optimizing embedded applications to reduce power consumption.

With: Robert Oshana

Wednesday, 9 March 2005

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ETP-369 Using ZigBee Technology for Low Power Device Designs

Level: Intermediate

ZigBee is a standards-based, low cost, low power technology that will enable the broad-based deployment of wireless networks in home, enterprise and industrial settings. The ZigBee protocol was designed to facilitate long-life battery applications. Devices can be powered either by battery or line, though ZigBee has always highlighted its battery-powered capabilities. This class describes the ZigBee specification and tells how to integrate ZigBee technology into various mobile device designs for low power functionality.

What You'll Learn: How to utilize the ZigBee protocol and other enabling technologies to design mobile devices.

Target Audience: Engineers, Designers and Managers looking for ways to extend battery life and utilize new networking technologies.

With: Jon Adams

Wednesday, 9 March 2005

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ETP-370 CANopen-Based Transducer Network

Level: Introductory

In order to reduce the integration effort that is necessary especially in sensor-intensive applications, the CAN in Automation (CiA) international users' and manufacturers' group has developed a CANopen device profile (DS 404) for transducers and closed-loop controllers that can be used to describe multi-sensor devices. Using this profile, the system designer can design cascaded networks. The multi-channel CANopen transducer module may use embedded communication links as defined in IEEE 1451. The CANopen devices provide compatibility to the Transducer Electronic Data Sheet (TEDS) as defined in IEEE 1451.

What You'll Learn: How to build simple and cascaded embedded networks, depending on the requirements, as proposed by IEEE 1451.

Prerequisites: General understanding of CAN networks required.

Target Audience: Engineers that have to setup communication structures based on embedded networks.

With: Cyrilla Menon

Wednesday, 9 March 2005
3:45pm - 5:15pm



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ETP-400 Multiprocessing in Embedded Systems

Level: Introductory

Embedded systems are constantly demanding more of the CPUs within them, and one way to efficiently design complex systems is by utilizing multiple CPU cores. This class provides an introduction to multiprocessing topics and covers both hardware and software requirements, with an emphasis on software development. Topics include different models of parallel programming, communication, synchronization, and a discussion of what is required of software engineers to utilize a multiprocessor system. The class also provides a survey of some currently available technologies.

What You'll Learn: Basic multiprocessing concepts to use when deciding whether to implement a multiprocessing system for a project.

Prerequisites: Familiarity with C useful.

Target Audience: Embedded systems software engineers and engineering managers receive an introduction to multiprocessing concepts that may aid in future project development.

With: Tracy Thomas

Thursday, 10 March 2005
8:30am - 10:00am



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ETP-401 Model Driven Development of Resource Constrained Embedded Applications

Level: Intermediate

Many embedded systems are constrained in the amount of memory and computational processing power available. The use of models to generate embedded applications requires thoughtful attention to these constraints. This class investigates the use of the Unified Modeling Language (UML) modeling tools for the generation of resource constrained applications. A small case study of an embedded system is used. Trade-offs in using high-level abstractions such as active objects are investigated. Productivity and quality gains from using models for embedded development are discussed.

What You'll Learn: UML for modeling resource constrained embedded systems, and how to minimize resource demands of the system under development while still using a model driven approach.

Prerequisites: Programming experience in C required, UML experience a plus.

Target Audience: Intended for SW developers and architects, challenged with developing real time embedded software for resource constrained systems with heavy time-to-market requirements.

With: Ton Janssen

Thursday, 10 March 2005
8:30am - 10:00am



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ETP-402 Fundamentals of Digital Imaging, Part 1

Level: Introductory

Digital imaging knowledge is important for devices with graphical displays and hard copy output capability. This class explores the fundamentals from capture to image processing through output. Topics covered include CCD/CMOS sensor interfacing, basic image processing, color spaces, and working with output devices such as display controllers and printers. Attendees will be able to answer the age old question "Why does it look so good on my screen and so bad when I print it out?" This is the first class in a two-part series.

What You'll Learn: An understanding of digital imaging devices, how to interact with image capture and output components, and the basics of optimizing image processing.

Target Audience: Embedded Software Developers

With: John Canosa

Thursday, 10 March 2005
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ETP-403 The Perils of FPGA Timing Closure

Level: Intermediate

Looking into the struggles to get large designs to closure can provide valuable insight to others using large FPGAs. This class describes a project involving three large FPGA designs, two in Xilinx V2 3000 parts, and one in a Xilinx V2 Pro 50, in which timing closure was not expected to be a problem. But it was. Techniques to be examined include area constraints, synthesis options, physical synthesis, par switches, "secret" par switches, and hierarchical floor planning.

What You'll Learn: Achieve timing closing by studying various techniques used on three large FPGA designs.

Prerequisites: Understanding of digital hardware design including hardware description languages, knowledge of FPGA features and architecture, and exposure to FPGA tool flows required.

Target Audience: Digital design engineers and managers involved in large FPGA designs. Designers using Xilinx FPGAs benefit most from the class since the examples are all related to Xilinx-based parts and flow.

With: Carl Christensen

Thursday, 10 March 2005
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ETP-404 Selecting Linux as an Embedded Operating System

Level: Introductory

There are significant tradeoffs to be made when selecting a suitable OS for any particular device. This class looks at the considerations when evaluating Linux as an embedded operating system, and shares some insights gained on a real project, during which, the promise of being able to use completely free, mainly open-source software and development tools was put to the test with a good measure of success. Attendees learn the issues associated with using Linux and other open source software in an embedded system.

What You'll Learn: How to evaluate whether Linux might be a suitable operating system to use in a future product.

Target Audience: Technical Managers, Team Leaders, System Architects

With: [Paul Knot](#)

Thursday, 10 March 2005
8:30am - 10:00am



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ETP-405 C++: Inheritance, Interfaces and Thunks

Level: Advanced

Since its standardization in 1998, C++ has grown as a plausible alternative to C as an embedded programming language. To date, many programmers have not used C++ Multiple Inheritance (MI) because it is not supported (e.g. Embedded C++) or because of concerns over the performance impact. However, with the acceptance of UML 2.0, the concept of multiple interfaces will play a much greater role in design, thus forcing the use of MI. This class looks at the real impact of using MI in an embedded design.

What You'll Learn: The memory and performance impact of using C++ multiple inheritance in an embedded system, the need for "thunks," and how to minimize overheads.

Prerequisites: Basic C++ experience required.

Target Audience: Embedded programmers currently using C++ who have either been using Embedded C++ (EC++), or shied away from using multiple inheritance because of the memory and performance overheads.

With: Niall Cooling

Thursday, 10 March 2005
8:30am - 10:00am



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ETP-406 Practical Statecharts for Embedded Systems, Part 1

Level: Intermediate

This class shows practical ways to use UML statecharts in designs, to help produce efficient and maintainable systems with well-understood behavior, rather than creating "spaghetti" code littered with convoluted ifs and elses. Part 1 presents the essence of statecharts, why are they fundamental, and how to practically code them directly in C or C++ without sophisticated CASE tools. Part 2 shows how to combine concurrent state machines into applications, presents a lightweight, portable event-driven framework for real-time embedded systems, and teaches how to build and use a minimal statechart-based application framework. This is the first class in a two-part series.

What You'll Learn: How to apply statecharts to construct more robust and maintainable event-driven software and how to practically code statecharts in C or C++.

Prerequisites: Fluency in C required, familiarity with inheritance in C++ a plus. Part 2 requires general understanding of preemptive multitasking, mutual exclusion, and blocking.

Target Audience: Embedded programmers and consultants; Real-time systems designers; Users of design automation tools

With: Miro Samek

Thursday, 10 March 2005

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ETP-407 Extreme Programming and Embedded Software Development

Level: Introductory

Extreme Programming (XP) made its debut in 1999. The topic is still a hot bed of discussion; much of that discussion is mired in rumor and misinformation. XP is an Agile software development methodology, iterative at its core and reducing development process overhead. This class explores the efficient and effective practices of XP and how to use it to develop embedded software. A team using XP makes concrete progress in embedded software development early in the development cycle, even prior to hardware availability.

What You'll Learn: How extreme programming and agile development can improve how you specify and develop software.

Target Audience: Embedded software developers, architects, team leads, managers, requirements engineers, project stakeholder, all those that have been disappointed by project delivery problems.

With: Robert C. Martin

Thursday, 10 March 2005
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ETP-408 Meeting RTCA/DO-178B/12B and ARINC 653 Safety Requirements for Critical Systems

Level: Advanced

This class reviews the DO-178B guidelines for software in airborne systems and equipment and discusses how equipment makers can bypass the labor-intensive certification process with commercial-off-the-shelf (COTS) solutions that use the standard ARINC 653 interface platform. It examines the typical architecture of a federated avionics system, analyzes the ARINC layer, and explains the advantages of integrated modular avionics (IMA). The class proposes a platform for software certification reuse that provides comprehensive software vulnerability analysis, is ARINC compliant and meets DO-178B certification evidence requirements.

What You'll Learn: Five levels of software defined by DO-178B, data documents required by DO-178B, and the requirements for an operating system to meet reusable software components approval.

Prerequisites: Familiarity with DO-178B and ARINC 653 standards helpful but not required.

Target Audience: Engineering managers, research and development engineers, design engineers, product engineers, military personnel, educators, students in the following industries: aerospace, government, NASA, Department of Defense, US Air Force, Independent consultants and contractors, academia

With: [Joe Wlad](#)

Thursday, 10 March 2005
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ETP-409 Hardware As Software: Designing with Configurable Processors

Level: Intermediate

This class examines configurable architectures which marry the flexibility of software programmability with the performance capabilities of ASIC designs in applications where SoC and ASIC design are economically infeasible and general purpose software processors can't meet minimum performance requirements. Software-configurable architectures blur the distinction between hardware and software. Key topics to be discussed include hardware/software partitioning issues, abstracting hardware as software, definition and use of custom instructions, designing for parallelism, dynamic adaptation to computational hotspots, and the management and optimization of simultaneous hardware/software design.

What You'll Learn: Configurable architectures and the impact this technology will have in future processor development.

Prerequisites: Familiarity with C and Assembly a plus.

Target Audience: Architect Engineering Managers and Systems Designers

With: Albert Wang

Thursday, 10 March 2005
8:30am - 10:00am



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ETP-410 Establishing Great Software Development Process(es) for Your Organization

Level: Introductory

There are many correlations between good software designs and good software development processes. It takes multiple views to adequately describe both software architectures and software development processes. One of the process views this class examines is a swim lane chart. This view highlights another parallel; good software designs limit the number of dependencies and interaction points between modules. The class introduces the traditional waterfall, incremental and iterative development models. A quick overview of a classic formal process (DoD-2167a) establishes a common reference for what artifacts are typically created under a formal process and touches on other factors that add to a project's complexity.

What You'll Learn: The elements that comprise a very formal software process and the ability to wisely select the pieces that are pertinent to your project.

Target Audience: Anyone tasked with, or wanting to, improve their company's development process. In particular, embedded developers that want to enhance the way their organization develops software.

With: [Dale Mayes](#)

Thursday, 10 March 2005
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ETP-420 Real-Time Architectures: Past, Present, and Future, Part 1

Level: Introductory

The architecture of response-time critical embedded systems is usually chosen early in the system's lifecycle. There are only four fundamental real-time architectural styles, each having its strengths and weaknesses. It is now known that a set of fundamental real-time architectural principles exists that govern these styles, and that can be exploited to successfully navigate this minefield throughout the system lifecycle. This class illustrates these four fundamental architectures, describes their strengths and weaknesses, and deals with the fundamental architectural concepts that could have strengthened them. This is the first class in a two-part series.

What You'll Learn: The fundamental real-time architecture styles, and the impact of using object-oriented architectures in embedded real-time systems.

Target Audience: Previous experience teaching similar material shows that participants at every experience level can derive immediate benefit constructing real-time applications.

With: Doug Locke, Mark Gerhardt

Thursday, 10 March 2005
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ETP-421 Real-Time Programming in Java

Level: Intermediate

By using the Real-time Specification for Java (RTSJ), developers can eliminate unpredictable latencies introduced by the garbage collector, exercise full control over thread priorities, and handle asynchronous events with ease. This class identifies the drawbacks of deploying conventional Java in a real-time system and how the RTSJ solves them. Using working code examples, we explore all the new classes that a Java Virtual Machine (JVM) supporting the RTSJ must provide. The class also examines how real-time behavior can be achieved via the Java Native Interface (JNI).

What You'll Learn: How to take advantage of the Real-Time Specification for Java.

Prerequisites: Experience writing application software in Java required.

Target Audience: Any embedded software developer that uses, or will use, Java in a system with real-time requirements.

With: [Steve Furr](#)

Thursday, 10 March 2005
11:15am - 12:45pm



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ETP-422 Fundamentals of Digital Imaging, Part 2

Level: Introductory

This is the second class in a two-part series. Please see class ETP-402 for abstract.

With: John Canosa

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ETP-423 Hardware/Software Codesign for Platform FPGAs

Level: Introductory

System-on-a-chip FPGAs including embedded processors, busses, memory, and hardware accelerators provide an opportunity to develop high performance, optimal systems. To realize the promise of this vision, a complete tool chain from concept to implementation is required. An automated design framework is described that allows development of hardware/software platform FPGA systems starting with a pure C design specification. Profiling, verification and advanced compilation technologies, including an optimized C to hardware compiler, provide a full push-button implementation flow.

What You'll Learn: How to develop platform FPGAs using a high-level software-centric flow.

Target Audience: System designers, embedded developers

With: Don Davis

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ETP-424 Bringing up a Custom Linux BSP

Level: Intermediate

Typical Linux makes extensive use of hardware MMUs and hardware services that were used only sparingly in legacy RTOS environments. In addition, Linux does not provide for boot firmware as part of the standard distribution. This class outlines the requirements for boot firmware interaction with the BSP as well as the steps required to get your board ready to start the Linux kernel. Strategies for building the BSP, placement of BSP-specific files, and the integration of that custom BSP into the Linux kernel sources are presented.

What You'll Learn: Knowledge of the Linux boot sequence and the role of boot firmware.

Prerequisites: Fluency in C required, understanding of CPU initialization techniques and make file syntax recommended.

Target Audience: This session is targeted to the engineer responsible for bringing Linux up on a custom processor board.

With: Michael Anderson

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ETP-425 High Assurance Java for Mission-Critical Systems, Part 1

Level: Intermediate

The safety-critical specification for Java (SCSJ) is designed to provide the high performance, small memory footprint, hard real-time determinism, and simplicity required for the development of DO-178B certified software in commercial and military avionics applications. Many of the special capabilities of the SCSJ are also well suited to development of high-assurance mission-critical software. This includes device drivers; interfaces to legacy software components written in C, C++, and Ada; and any software components that have demanding performance, footprint, or hard real-time determinism constraints. This is the first class in a two-part series.

What You'll Learn: Create architectures using the safety-critical specification for Java, and combine safety-critical components with traditional Java components in high assurance mission-critical systems.

Target Audience: Software engineers who need to apply the high-level benefits of Java to low-level mission-critical software including device drivers; components with demanding performance, footprint, or hard real-time constraints; interfaces to legacy components written in C, C++, or Ada; and systems that must be safety certified according to DO-178B guidelines.

With: Kelvin Nilsen

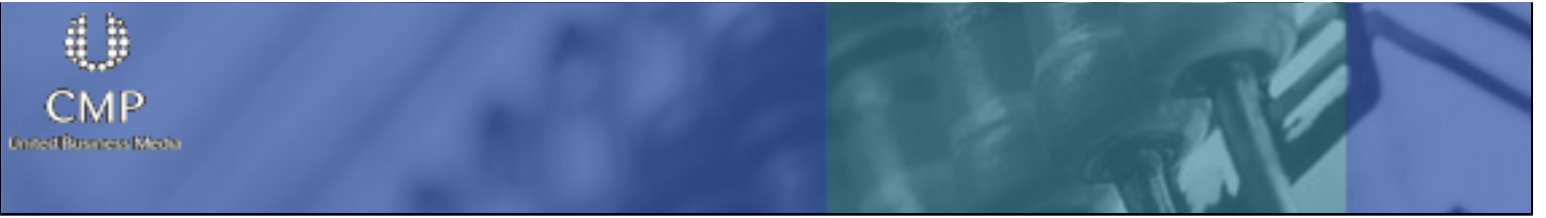
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ETP-426 Practical Statecharts for Embedded Systems, Part 2

Level: Intermediate

This is the second class in a two-part series. Please see class ETP-406 for abstract.

With: Miro Samek

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ETP-427 Debugging Embedded Linux Systems

Level: Intermediate

Despite their limitations, the simple flat-memory models of legacy home grown and commercial embedded operating systems are usually easy to debug. Debugging an embedded Linux system, where MMU translations are enabled and context switches across user modes are permitted at any time, requires new methods. This class discusses the challenges of debugging multi-threaded embedded Linux applications as well as the Linux kernel and device drivers. Techniques for debugging individual threads, processes, loadable kernel modules, and new hardware are presented.

What You'll Learn: Techniques for debugging multi-threaded embedded Linux applications, the Linux kernel, and device drivers.

Target Audience: Software developers, engineering managers and system architects benefit from this session.

With: Darcy Wronkiewicz

Thursday, 10 March 2005

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ETP-428 Safety-Relevant Communication in Embedded Control Systems

Level: Intermediate

The class introduces the CANopen Safety Protocol (CiA DS 304) and discusses the concept of serial redundancy transmitting safety-relevant data in two continuous messages with bit-wise inverted content. It also describes several implementation possibilities including a single-processor implementation done by a consortium of device manufacturers and system designers as well as configuration possibilities and restrictions. Using the generic profiles (I/O, motion control, encoder, and hydraulics) and some specific application profiles (e.g. lift and door control) in conjunction with the CANopen Safety protocol is covered.

What You'll Learn: How to realize safety-relevant communication on top of non-safety-relevant bus systems like CAN and CANopen.

Prerequisites: Understanding of digital hardware design required. General understanding of CAN networks a plus.

Target Audience: Decision makers and system developers with basic technical background in CAN that need to design systems with requirements for safety-relevant communication as required in medical systems and cutting machinery for example.

With: Cyrilla Menon

Thursday, 10 March 2005
11:15am - 12:45pm



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ETP-429 Integrating the Trusted Platform Module into Embedded Systems

Level: Intermediate

This class introduces the Trusted Platform Module (TPM), its capabilities, the Message Communication protocol, RSA basics, and details the TPM Key Hierarchy. The class details a methodology that enables successful integration of the TPM into a design and provides the methodology for verifying the TPM's operation on a specific platform.

What You'll Learn: Trusted Platform Module specification, capabilities for embedded systems, and integration.

Target Audience: Embedded developers and designers.

With: Kevin Schutz

Thursday, 10 March 2005
11:15am - 12:45pm



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ETP-430 A Skills List for Developing Embedded Software

Level: Introductory

Developing software for embedded systems is inherently different than developing software for desktop or server environments. In this era of point-and-click, automated development, embedded development skills are becoming less common. This class helps traditionally trained software developers transition into embedded development, by giving an overview of the topics that they may need to spend time reviewing or learning. It provides a "study list" for engineers transitioning to the embedded realm, and also a "qualifications list" for managers looking to hire embedded developers.

What You'll Learn: Skills necessary to transition from traditional software development to embedded development.

Target Audience: Engineers and Managers starting Embedded development for the first time.

With: Dale Word

Thursday, 10 March 2005

11:15am - 12:45pm



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ETP-440 Real-Time Architectures: Past, Present, and Future, Part 2

Level: Introductory

This is the second class in a two-part series. Please see class ETP-420 for abstract.

With: Doug Locke, Mark Gerhardt

Thursday, 10 March 2005
2:00pm - 3:30pm



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ETP-441 Measuring and Tuning Real-Time Performance of Embedded Systems

Level: Intermediate

Embedded systems often have performance bottlenecks, which prevent them from meeting their performance requirements. This class explores techniques to profile the system and presents data that can be extracted from the profiles allowing designers to identify bottlenecks and modify the design. The class presents real life examples. One of the case studies will be low bit rate speech encoders. We walk our audience through several changes in the design and their impact. Finally we show the tuned design achieving much lower frequency, saving power and cost.

What You'll Learn: Techniques to measure and improve the overall real-time performance of embedded systems.

Prerequisites: Familiarity with real-time hardware design issues helpful.

Target Audience: Designers and embedded system integrators, interested in measuring and optimizing the real time performance of the embedded system.

With: Rajat Moona, Russell Klein

Thursday, 10 March 2005

2:00pm - 3:30pm



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ETP-442 Software Defined Radio with Reconfigurable Hardware and Software

Level: Introductory

This class presents a step-by-step walk through of the implementation of a Software Defined Radio (SDR) system running on embedded Linux in a single FPGA. We discuss aspects of hardware and software partitioning between the FPGA fabric and the embedded processors as well as between the processors themselves and show the advantages of Software Defined Radio on reconfigurable computing systems over existing solutions. The result is a working SDR application using hardware, software, and a full embedded operating system.

What You'll Learn: Development process for hardware/software platform, including tools and target platforms.

Target Audience: Hardware, firmware and embedded engineers

With: Peter Ryser

Thursday, 10 March 2005
2:00pm - 3:30pm



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ETP-443 Model-Based Design of Closed Loop Control for Embedded Systems Using Fixed Point Controllers

Level: Intermediate

This class shows the application of Model-based design to the development of a closed-loop, real-time motor control application. The system was modeled as a block diagram; different pieces of the system are simulated to validate algorithms using 32-bit fixed-point operations. Automatic code generation was used to verify performance on a fixed point DSP controller. The algorithms are presented in detail, and the accuracy of 32-bit fixed-point operations is compared with 16-bit fixed point and floating-point operations. The comparison results show that proper 32-bit fixed-point operations provide excellent performance for any embedded system implementations.

What You'll Learn: Achievement of system-level optimizations which can be difficult to realize using only C or HDL-based tools.

Target Audience: DSP engineers

With: Arefeen Mohommad, Zijad Galijasevic

Thursday, 10 March 2005
2:00pm - 3:30pm



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ETP-444 Power Management Strategies in Embedded Applications, Part 1

Level: Intermediate

Low-power techniques are increasingly important for portable embedded applications. This class introduces software and hardware approaches for aggressively managing the power budget. Implementation of a range of reduced-power modes between fully on and fully off is discussed, with reference to support for these modes in communication protocols and embedded controller silicon.

What You'll Learn: Understanding of low-power options and techniques to maximize portable designs.

Prerequisites: Basic understanding of IC and board level power consumption required.

Target Audience: Intermediate designers and engineers

With: [Gordon Mortensen](#)

Thursday, 10 March 2005
2:00pm - 3:30pm



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ETP-445 High Assurance Java for Mission-Critical Systems, Part 2

Level: Intermediate

This is the second class in a two-part series. Please see class ETP-425 for abstract.

With: Kelvin Nilsen

Thursday, 10 March 2005
2:00pm - 3:30pm



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ETP-446 Data Management for Highly Available Embedded Systems

Level: Intermediate

The class introduces the field of highly available databases (HA DBs). The required availability level of contemporary telecom systems is around "5 nines," that is 99.999% availability. A special challenge of HA DB systems is that the pure availability of the service is not sufficient--the integrity of the data has to be maintained over any failure scenario. An overview of commercially available architectures is given, together with guidelines to various trade-offs achieved with the technology. The criteria for and behavior of a HA DB compliant with the SA Forum's specifications is described.

What You'll Learn: Selecting an appropriate database product, choosing between alternative high-availability database technologies, and the Service Availability Forum's AIS (Application Interface Specification.)

Target Audience: The target audience is programmers, project managers and architects aiming at developing data intensive embedded products.

With: Ali Paasimaa

Thursday, 10 March 2005
2:00pm - 3:30pm



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ETP-447 Covering Multiple Embedded Networking Technologies with CANopen

Level: Intermediate

This class explains how embedded communication methods can share a common network protocol, providing a transparent network protocol covering several layers in an embedded networking system. The hardware layers unified by this method include UART, LIN, I2C, CAN and Ethernet. The general, shared CANopen functionality required for such a hardware-independent implementation is summarized in this class followed by a review of how this technology is adapted for the different hardware layers. The class ends with an overview of the general requirements that other physical layers must meet to be usable for CANopen.

What You'll Learn: How CANopen can be used on multiple network technologies, including I2C, UART, LIN, CAN and Ethernet.

Prerequisites: General knowledge about embedded networking required.

Target Audience: Engineers and Managers that use or consider using embedded networking - communication between multiple embedded devices

With: Christian Keydel, Olaf Pfeiffer

Thursday, 10 March 2005
2:00pm - 3:30pm



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ETP-448 Building Internet Applications with Microsoft's .NET Compact Framework

Level: Intermediate

This class describes the benefits of writing Internet-enabled mobile and wireless applications for Windows CE using the Microsoft .NET Compact Framework. The .NET Compact Framework and the tools available for building applications using the framework are explained. The Microsoft .NET Compact Framework is compared to the traditional Win32 approach to writing such applications for Windows CE. Attendees will be able to start writing their own web applications for platforms such as the Pocket PC and Smart Phone immediately.

What You'll Learn: Ability to create Internet-enabled applications for a variety of Windows CE devices and platforms using the Microsoft .NET Compact Framework.

Prerequisites: Some experience with Windows or Windows CE application programming and C or C++ programming required. C# or vb.NET programming a plus.

Target Audience: This session is aimed at intermediate level application and systems programmers looking to explore the benefits of using Windows CE and the Microsoft .NET Compact Framework to build mobile and wireless web-connected applications

With: Robert Burdick

Thursday, 10 March 2005

2:00pm - 3:30pm



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ETP-449 Application Development for ZigBee Wireless Networking

Level: Introductory

ZigBee addresses networking among devices with low-data rate exchange needs, such as lighting, HVAC, security, medical and other monitoring and control applications using sensors and actuators. This class covers the basics about the ZigBee wireless networking standard, including the various layers of the stack, and the application framework and profiles, which assure interoperability and form an application foundation. Considerations in writing a ZigBee application are discussed while examining C source code for a simple application. A ZigBee wireless network will demonstrate the application in use.

What You'll Learn: ZigBee basics, including the PHY and MAC layers, and the ZigBee stack.

Target Audience: The target audience is any programmer that is interested in writing ZigBee wireless applications for low-cost, low-power, low-data rate, high-security, and high reliability devices, most of which use 8 bit microprocessors.

With: [Drew Gislason](#)

Thursday, 10 March 2005
2:00pm - 3:30pm



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ETP-450 The Hardware/Software Co-design for Road Vehicle Control System

Level: Intermediate

In vehicle control systems electric control unit (ECU) as software content grows, appropriate MCU loading becomes difficult to maintain. One path to successful development is to use co-design for the control system. In this class we focus on how to apply the co-design to the problem. We propose a co-design environment, applying high-level synthesis. By applying co-design to the engine ECU, we succeeded in transforming part of the software into custom hardware, thus reducing the load on the target MCU.

What You'll Learn: How to apply co-design to vehicle control system applications.

Prerequisites: Understanding of system level design required. C programming experience for control system required. Knowledge of digital hardware architecture required.

Target Audience: The following can get a lot of benefit from this session. The system designers and software engineers of embedded system who want to use the co-design tool. The co-design tool providers. In addition to them, the following can get the benefit, too. The software environment providers. The semiconductor(include FPGAs) manufacturers.

With: [Ryuji Okamura](#)

Thursday, 10 March 2005
2:00pm - 3:30pm



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ETP-460 Complementing DSPs with FPGAs

Level: Intermediate

A new generation of low-cost FPGAs can be used to resolve system-level challenges without significantly impacting overall system costs. These FPGAs can be used to implement peripherals, replace hard-to-find components, connect high-speed analog-to-digital and digital-to-analog converters, streamline data transfers, act as co-processors or fill any other gap between the end application and the system designer's DSP of choice. This class describes real-world situations where system-level challenges require a solution involving more than just a DSP. In each example, the benefits of partitioning the system between a DSP and an FPGA are detailed.

What You'll Learn: Confidence in suggesting a DSP + FPGA solution when customers run into roadblocks using a DSP by itself.

Prerequisites: Basic FPGA technology knowledge required.

Target Audience: 1) Applications engineers interested in learning how system problems can be solved by partitioning a problem between a DSP and a FPGA 2) Sales representatives looking for a high level understanding of where FPGAs fit in a TI centric design 3) Experienced engineers looking for a demo of how current tool sets allow FPGAs to be connected to a TI DSP with relative ease

With: Paul Ekas

Thursday, 10 March 2005
3:45pm - 5:15pm



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ETP-461 Scalable and Platform Agnostic Device Driver Architecture

Level: Intermediate

As new operating systems and hardware platforms emerge, device driver development and validation becomes more demanding. Duplicate efforts appear in device drivers that support a combination of software/hardware platforms. Good modularization and layered functional abstraction practices help produce scalable and portable device drivers that reduce the maintenance costs while improving the adaptability for future OS and hardware platforms. This class discusses the pros and cons of a modular driver framework vs. a traditional device driver development model.

What You'll Learn: Learn the importance of strong software engineering principles like modularity, reusability, and scalability.

Prerequisites: Device driver programming experience and fluency in C required. Graphics driver knowledge a plus.

Target Audience: This session will best benefit device driver developers, especially those with development experience in traditional monolithic models that is limited to a single hardware and OS combination. This material provides architecture guidelines to develop a code base that scales farther across families of hardware platforms and Operating Systems such as in the case of multiple generations of a vendors graphics chips on Linux and Windows family of OS.

With: Matthew Sottek

Thursday, 10 March 2005
3:45pm - 5:15pm



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ETP-462 MCUs for Motor Control

Level: Intermediate

This class introduces 3-phase electric motor basics and describes the various speed and torque control methods used to tackle the need for fast and precise motor response. Special peripherals such as 6-phase PWM timers, synchronized fast ADC, encoder timers and high performance CPUs with programmer friendly architectures are key features for modern motor-control MCUs. They can greatly reduce the software overhead and allow real-time processing of sensor signals, as well as the implementation of sophisticated control algorithms, yet leave enough room for other system tasks such as managing communication or human interface.

What You'll Learn: Basic MCU features and the implementations of various speed and torque control methods for more energy efficient appliances.

Prerequisites: Basic understanding of microcontroller architecture and digital electronics required. Knowledge about motors and motor control a plus.

Target Audience: Embedded systems engineers interested in developing motor-control applications will benefit the most from this session.

With: John Pocs

Thursday, 10 March 2005
3:45pm - 5:15pm



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ETP-463 Integrating DSP Design and Test for Rapid Product Development

Level: Intermediate

Due to the complexity and variety of DSP applications, testing DSP algorithms with various parameters can be challenging. LabVIEW graphical development provides a rapid platform to develop, debug, and test applications through RTDX. Furthermore, the LabVIEW DSP Test Integration toolkit provides a plug-in to the Texas Instruments Code Composer Studio IDE to debug DSP algorithms without needing to program. This class walks through how companies in automotive and aerospace are using LabVIEW and Code Composer Studio to reduce the development time for their audio, video, and control applications.

What You'll Learn: Decrease time to market by testing software and hardware earlier in the design process.

Target Audience: DSP software engineers looking for additional ways to decrease their time to market through new testing strategies. Typically, these engineers will be frustrated by the inefficiencies brought on by needing to wait for hardware prototype in order to test code.

With: Mike Trimborn

Thursday, 10 March 2005
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ETP-464 Power Management Strategies in Embedded Applications, Part 2

Level: Intermediate

This is the second class in a two-part series. Please see class ETP-444 for abstract.

With: Gordon Mortensen

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ETP-465 Secure Safety-Critical Distributed Embedded Systems

Level: Intermediate

To address the need for security in embedded and real-time systems, an architecture based on a small separation, or partitioning, kernel has been proposed termed the MILS (Multiple Independent Levels of Security). The architecture classifies the components of a system into three layers; the partitioning kernel, the middleware, and the application layer. The class discusses the MILS architecture, its impact upon current and future embedded system development, and the certification process.

What You'll Learn: The architecture of MILS systems and the design goals behind MILS, MILS Middleware and MILS Systems.

Prerequisites: Working understanding of computer systems required.

Target Audience: Developers who will be working with secure, safety-critical embedded systems. With an emphasis on developers who are concerned with ARINC-653 and DO-178B systems.

With: Bill Beckwith, Joseph Jacob, Mark Vanfleet

Thursday, 10 March 2005
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ETP-466 Introduction to the PowerPC Programming Model

Level: Intermediate

As CISC programmers transition from legacy processors to RISC architectures such as the PowerPC, they are faced with a steep learning curve. This class presents an overview of the PowerPC programming model for engineers and programmers who are new to the PowerPC architecture. The class discusses the PowerPC storage model, registers, instruction types and formats, memory management, interrupt handling, debug facilities, and provides suggestions for maintaining code compatibility across different PowerPC implementations.

What You'll Learn: PowerPC architecture from a programming perspective, along with its components and instructions.

Prerequisites: Some assembler or C programming experience required.

Target Audience: Engineers, programmers and managers who are new to the PowerPC architecture, assigned to projects using PowerPC or investigating the potential usefulness of the PowerPC Architecture.

With: Paul Gramann

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ETP-467 Emerging Landscape of High Speed Serial Interconnect Standards

Level: Introductory

To alleviate the problems of high cost, long lead times, and lack of interoperability of proprietary high speed interconnects, several industry forums have sprung up to unleash new serial high speed interconnect standards and protocols. The contenders include: Serial Rapid IO, PCI Express, Advanced Switching (an extension of PCI Express), and Backplane Ethernet. Latencies, congestion management, quality of service, redundancy, and high availability are some of the features that will play decisive roles in this competition. This class discusses and compares the strengths and weaknesses of the underlying technology and ecosystem of the competing high speed interconnect standards to understand their future prospects.

What You'll Learn: Technological strengths and weaknesses of the high speed interconnect standards.

Target Audience: System hardware/ software engineers in specific and engineering and marketing managers in general will benefit the most from the presentation.

With: Harpinder Matharu

Thursday, 10 March 2005
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ETP-468 Bridging Embedded Network Technologies

Level: Intermediate

This class summarizes common communication methods used and focuses on the requirements for a bridge application, where multiple communication methods and layers come together in a single chip. The different network layers typically used in embedded applications are summarized and evaluated. Network technologies covered include I2C, UART, LIN, CAN and Ethernet. The evaluation also includes a comparison of regular implementations versus smart implementation of these technologies. Using a Philips LPC2000 ARM7TDMI microcontroller, a real-world bridge example is demonstrated.

What You'll Learn: What to pay attention to when using a single microcontroller to bridge multiple communication networks including I2C, UART, LIN, CAN and others.

Prerequisites: General knowledge about embedded networking and/or CANbus required.

Target Audience: Engineers and Managers that use multiple communication technologies in their embedded applications

With: Axel Wolf, Olaf Pfeiffer

Thursday, 10 March 2005

3:45pm - 5:15pm



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ETP-469 The Joy of Real-Time Artificial Intelligence

Level: Introductory

Combining real-time systems with AI is like combining chocolate ice cream with onions. They just doesn't mix well together. The purpose of this class is to explore the problems of applying AI techniques to real-time systems, or, applying real-time requirements to AI systems. A historical perspective will be given which will carry through to the present to show the evolution of real-time AI systems. Real-world examples will be given.

What You'll Learn: Understanding the problems inherent in combining AI and real-time systems.

Target Audience: I think the best audience will be one that is curious about this somewhat obscure topic. Researchers and scientists who enjoy exploring alternate solutions to problems would also benefit. Also, this would be interesting and fun for anyone who was involved in AI in the mid to late eighties and would like to see how real-time systems have evolved into the AI equation since then.

With: [Mikel Cvetanovic](#)

Thursday, 10 March 2005
3:45pm - 5:15pm



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ETP-470 Safety Critical Software Verification: Lessons From the DO-178B Approach

Level: Intermediate

Published by Requirements and Technical Concepts for Aviation Inc., the DO-178B Software Considerations in Airborne Systems and Equipment Certification document offers guidelines that are unique relative to other quality processes, because they state that the verification activities used for a given system should be determined by how safety critical the system is. This class looks at what is meant by the term "software quality," and then reviews validation and verification activities. Finally, we describe three powerful software verification lessons and a golden rule that you can start implementing today.

What You'll Learn: Improve software quality by studying code quality standards and guidelines used by the FAA to certify safety critical avionics systems.

Prerequisites: C, C++ or Ada programming experience required, software test experience a plus.

Target Audience: Software developers and software validators/testers

With: Todd Greenwalt

Thursday, 10 March 2005
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Mikel Cvetanovic

Principal Software Engineer
Raytheon Company

Mikel Cvetanovic has spent almost 20 years designing and implementing real-time AI systems, transaction processing systems, control systems, help desk systems, advanced e-commerce solutions and driver development. Cvetanovic has also programmed in many languages to include C, C++, Ada, PL/I, Forth, Lisp, Pascal, Basic, Cobol, Prolog, Smalltalk, Assembly, etc. Currently, Cvetanovic is working in a systems engineering capacity overseeing large real-time systems projects. He holds a BSCE, and an MSCS.

Classes:

ETP-469 - The Joy of Real-Time Artificial Intelligence

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The Embedded Training Program 2005 Proceedings

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